5005 5006
Service Manual

Courtesy of:-

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5005
5006
DIGITAL MULTIMETERS

RACAL-DANA

RACAL-DANA INSTRUMENTS INC.
18912 Von Karman Ave., Irvine, CA 92715
Telephone: 714/833-1234, TWX: 910-595-1136, TLX: 67-8341

RACAL-DANA INSTRUMENTS LTD.
Duke Street, Windsor, Berkshire SL4 1SB, England
Telephone: Windsor (07535) 69811, TLX: 847013

RACAL-DANA INSTRUMENTS S.A.
91 Route de Gardes, 92 Meudon-Bellevue, France
Telephone: (1) 534-7575, TLX: 200207

RACAL-DANA INSTRUMENTS, LTD., DEUTSCHLAND
Hermanstrasse 29, D-6078 Neu Isenburg, Federal Republic of Germany
Telephone: 06102-2861-2, TLX: 412896

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WARRANTY

Within one year of purchase, Racal-Dana will repair or replace your instrument, at our option, if in any way it is defective in material or workmanship. All parts and labor charges will be paid by Racal-Dana Instruments. Just call Racal-Dana Product Service at (714) 833-1234 in U.S.A., Windsor (07535) 69811 in England, 027-7575 in France, or 06102-2861/2 in Germany for assistance. We will advise you the proper shipping address for your prepaid shipment. Your instrument will be returned to you freight prepaid.

PROPRIETARY NOTICE

FOR YOUR SAFETY

Before undertaking any maintenance procedure, whether it be a specific troubleshooting or maintenance procedure described herein or an exploratory procedure aimed at determining whether there has been a malfunction, read the applicable section of this manual and note carefully the WARNING and CAUTION notices contained therein.

The equipment described in this manual contains voltage hazardous to human life and safety and which is capable of inflicting personal injury. The cautionary and warning notes are included in this manual to alert operator and maintenance personnel to the electrical hazards and thus prevent personal injury and damage to equipment.

If this instrument is to be powered from the AC line (mains) through an autotransformer (such as a Variac or equivalent) ensure that the common connector is connected to the neutral (earthed pole) of the power supply.

Before operating the unit ensure that the protective conductor (green wire) is connected to the ground (earth) protective conductor of the power outlet. Do not defeat the protective feature of the third protective conductor in the power cord by using a two conductor extension cord or a three-prong/two-prong adapter.

Maintenance and calibration procedures contained in this manual sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures carefully and heed Warnings to avoid "live" circuit points to ensure your personal safety.

Before operating this instrument.

1. Ensure that the instrument is configured to operate on the voltage available at the power source. See Installation section.
2. Ensure that the proper fuse is in place in the instrument for the power source on which the instrument is to be operated.
3. Ensure that all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If at any time the instrument:

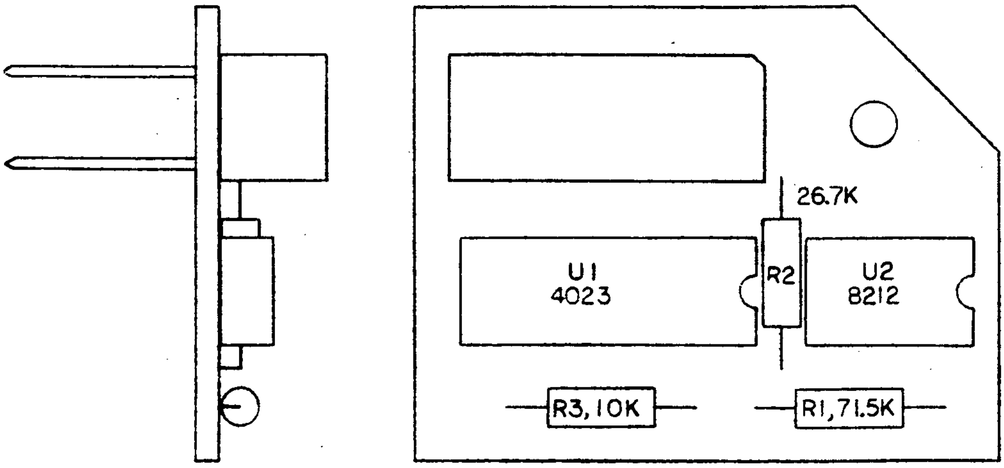
- Fails to operate satisfactorily
- Shows visible damage
- Has been stored under unfavorable conditions
- Has sustained stress

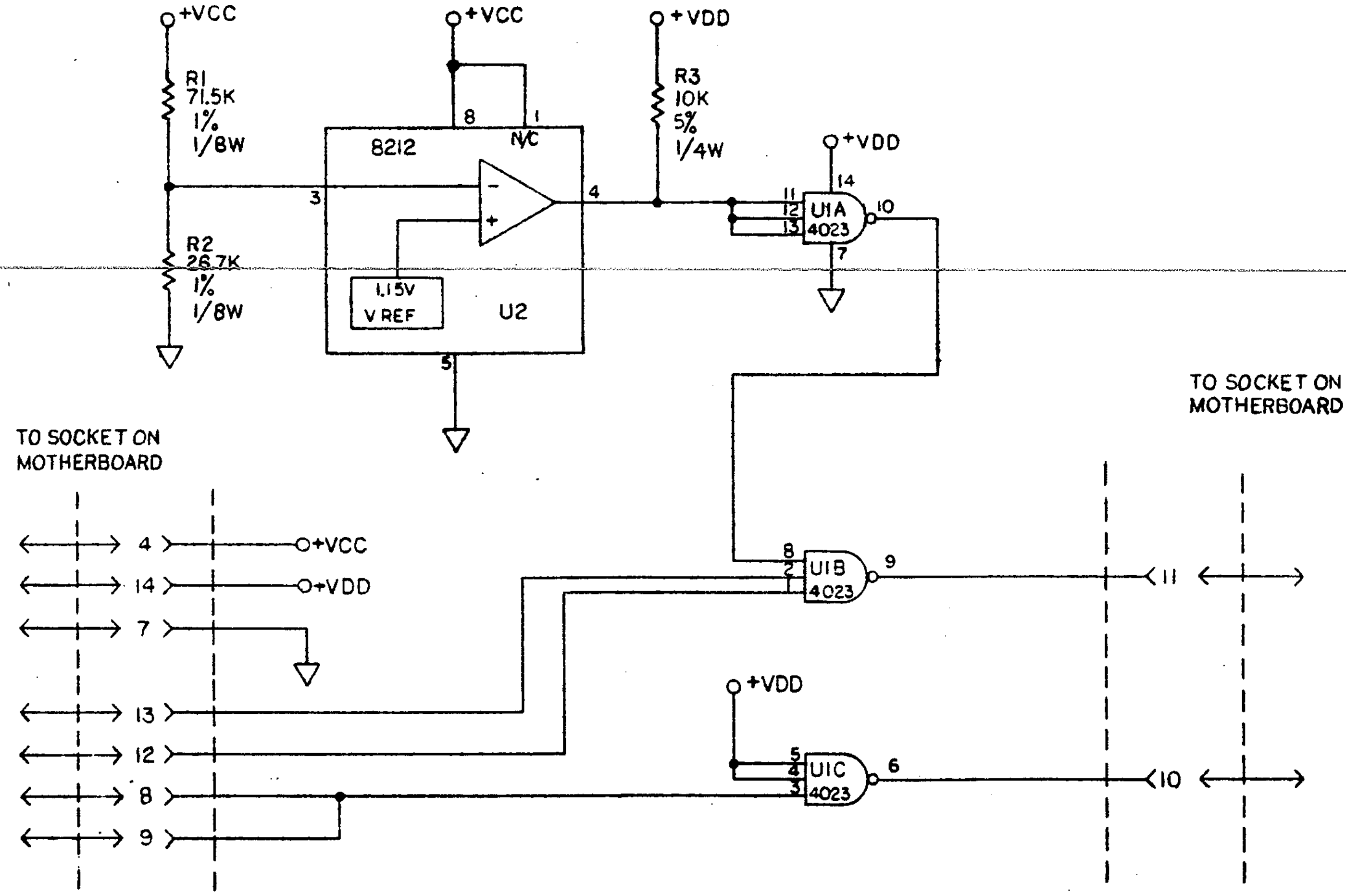
It should not be used until the performance has been checked by qualified personnel.

ADDENDUM

October 20, 1981

On Motherboards up to revision H, a plug-in assembly P/N 401683 replaces U42.





401683 - PCB Assy, NON-VOL, PWR. DOWN

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
R3	000103	RES CARBON 10K 5% 1/4W	81349	RC07GF103J
R1	010643	RES METAL 71.5K 1% 1/10W	81349	RN55C7152F
R2	010697	RES METAL 26.7K 1% 1/10W	81349	RN55C267F
U2	230515	IC MICROPOWER VOLTAGE DETECTOR	32293	ICL8212CPA
U1	230588	IC CMOS TRIPLE 3 INPUT NANDGATE	27014	CD4023C

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SECTION 1 GENERAL DESCRIPTION

1.1 PURPOSE.

1.1.1 Racal-Dana Instruments prepared this Instruction Manual for the Micro 5000 Series Digital Multimeter (DMM). The manual provides the user with the operating procedures necessary to employ the features designed into the instrument. Also, the manual details the calibration and maintenance procedures required by technical people to obtain the maximum performance specified by Racal-Dana in the published specifications. It is recommended that the users and technicians read this manual before operating the instrument.

1.2 SCOPE.

1.2.1 The Instruction Manual presents the information for the Models 5005 and 5006 concurrently as one throughout the manual. Special attention is given to the features that are unique to each model as the subjects are presented in context. The sections in the manual include: General Description, Installation, Operation, Theory of Operation, Maintenance, Drawings and Parts List.

1.3 PRODUCT SUPPORT GROUP.

1.3.1 The Racal-Dana Irvine complex maintains a complete Engineering laboratory, Field Engineers, service department and parts department to support the product commitment. Further support is provided by a network of area service centers and Field Representatives, the complete list appears on the last two pages of the manual. The warranty program declaration is presented in the forward section of this manual, also service personnel are available for service consultation.

1.4 ELECTRICAL DESCRIPTION.

1.4.1 The Racal-Dana Model 5005 or 5006 microprocessor (μP) based digital multimeter (DMM) is a 5-1/2 digit auto-ranging multimeter. The basic functions include 5 DC volt scales ranging from 0.1 volt to 1 KV; 4 AC volt scales ranging from 1 volt to 1 KV, and 6 resistance measurement scales ranging from 0.1K ohm to 10,000K ohms. The chart in Table 1.1 represents the DMM function and ranges. For systems applications, the Model 5005 or 5006 features an IEEE-488-1978 (GPIB) interface.

1.4.2 The DMM measurement process depicted in the block diagram Figure 1.1 consists of three major parts:

Table 1.1 - DMM Function and Range

RANGE	FUNCTION: DC	AC	OHMS
.1V	■		
1V	■	■	
10V	■	■	
100V	■	■	
1000V	■	■	
.1KΩ			■
1KΩ			■
10KΩ			■
100KΩ			■
1000KΩ			■
10000KΩ			■

a) The Signal Conditioning section where the input signal is switched, scaled, attenuated, rectified and filtered under microprocessor control.

b) The Analog-to-Digital converter employs a Quantized Feedback conversion technique, to change the DC voltage into a representative digital signal.

c) The μP-based digital section translates the analog to digital (A/D) converter output to a numerical value for the instrument display and GPIB output that represents the value of the input signal. The digital section also provides function selection, range control, decimal placement and programming.

1.5 MECHANICAL DESCRIPTION.

1.5.1 The DMM physical configuration is outlined in Figure 1.2, a dimensional outline projecting the front and rear views from the top elevation. The front panel contains the keyboard switches, the LED display, and Input terminals. The rear panel contains Input terminals, 24 pin GPIB connector, GPIB address switch, two BNC connectors, 3 prong AC power plug and fuse.

1.6 POWER REQUIREMENTS.

1.6.1 The DMM is designed to operate from a wide range of AC line voltages and frequencies with 120 VAC and 60 Hz considered standard. The selectable multi-tapped primary winding will accommodate line voltages of 100,

Table 1.2 - Specifications

GENERAL SPECIFICATIONS	
Power Requirements:	100, 120, 220 or 240 ± 10% 25 Watts maximum 60 Hz Standard 50 Hz Available
Weight:	15 lbs.
Dimensions:	3.5" Height x 14" Deep x 16.6" Wide
Rack Mounting:	Standard Corporate Package
Warranty:	Standard Warranty Statement
Temperature Range: Operating Storage	 0°C to 50°C –40°C to +70°C @ 80% R.H.
Humidity, Operating:	< 75% RH; 0°C to 40°C < 50% RH; 40°C to 50°C
Fuse:	.5 Amp "Slo-Blo" (115V) .25 Amp "Slo-Blo" (220V)
Battery:	A 3.0V lithium battery provides power for the non-volatile memory whenever the DMM is turned off. Battery life is 3 years minimum at a 50° C ambient temperature. Battery is not rechargeable.

DMM GENERAL	
Data Display:	5 full decades plus overrange digit in 5-1/2 digit mode. 4 full decades plus overrange digit in 4-1/2 digit mode.
Overload Indication:	Display reads "OL".
Warmup Time to 24 hr. Specifications:	2 hours.
Warmup Time to Fully Stabilize to 6 mo. Specifications:	1 hour.
Maximum Common Mode Voltage:	1000V peak or DC, Guard to case. 250V Peak or DC, Analog Common to Guard.
Overrange:	100% overrange with full accuracy on all ranges and functions except 1KV (1000V DC or 1500V peak AC max.)
Ranging:	Autorange standard Upranges at approx. 225% of range. Downranges at approx. 20% of range. Manual range standard.

DMM GENERAL continued	
Read Rate: * **(Internal Trigger, External or GPIB Trigger)**	4 Readings/Sec in 5-1/2 digit mode (60 Hz instrument). 3.3 Readings/Sec (50 Hz instrument).
Timeout Delays: These delays are inserted between each ranging required during autorange and before the final reading.	DC 30 mS .1 KΩ to 1000 KΩ 40 mS 10,000 KΩ 300 mS AC 400 mS Any function with FILTER selected 500 mS
Autorange Delay:	See Timeout Delays above.
Filter:	Selectable 3-Pole active filter. Filter response is ≥35 dB down at 50 Hz (≥37 dB down at 60 Hz), attenuating 18 dB per octave above 60Hz to –60 dB or greater.

DC FUNCTION	
Ranges:	0.1, 1, 10, 100, 1 KV.
Resolution:	0.001% of Range in 5-1/2 digit mode (1 μV on 0.1V Range). 0.01% of Range in 4-1/2 digit mode (10 μV on 0.1V Range).
Maximum Input Voltage:	± 1000V DC or peak AC.
Accuracy, Short Term, 5-1/2 Digit Mode (after DIGITAL ZERO Command):	24 hrs., 23°C ± 1°C ±(0.007% Rdg + 3 digits).
Accuracy, 6 months, 23°C ± 5°C, 5-1/2 Digit Mode (after DIGITAL ZERO Command):	1V Range: ±(0.01% Rdg + 6 digits) Other Ranges: ±(0.02% Rdg + 6 digits)
Temperature Coefficient, 5-1/2 Digit Mode (after DIGITAL ZERO Command at new temperature):	±(0.0003% Rdg + 1 digit)/°C
Input Resistance:	0.1, 1, 10V Ranges: ≥ 1000 Megohms 100, 1 KV Ranges: 10 Megohms

* See p. 1-5 for 4½ Digit Mode Specifications

Table 1.2 - Specifications continued

DC FUNCTION continued	
Input Bias Current (at time of calibration):	≤ 50 pa at 23°C ± 1°C
Input Bias Current T.C.:	≤ 10 pa/°C
Normal Mode Rejection Ratio: Unfiltered	60 dB at 60 Hz (50 Hz on 50 Hz instruments).
Filtered	95 dB at 60 Hz 90 dB at 50 Hz on 50 Hz instruments.
Common Mode Rejection Ratio with up to 1 KΩ in either lead:	140 dB at DC 120 dB at 60 Hz (50 Hz on 50 Hz instruments).
Readout Noise:	0.1V Range: ≤ 4 digits p-p Other Ranges: ≤ 3 digits p-p.
Settling Time with up to 10 KΩ Source Resistance: (unfiltered)	0.1V Range: 10 ms to within 10 digits of final value. 1V, 10V Ranges: 5 ms to within 10 digits of final value. 100V, 1 KV Ranges: 10 ms to within 20 digits of final value.
Settling Time with up to 10 KΩ Source Resistance: (filtered)	470 ms to within 10 digits of final value.

OHMS FUNCTION	
Ranges:	0.1, 1, 10, 100, 1000 and 10,000 KΩ
Measurement Scheme:	Modified 4-Wire.
Voltage Across Unknown (Approx.):	–1V at F.S. –2V at 100% overrange.
Open Circuit Voltage:	–6V DC maximum.

OHMS FUNCTION continued	
Current Through Unknown (Approx.):	Range — Current .1 KΩ — 10 ma 1 KΩ — 1 ma 10 KΩ — 100 μa 100 KΩ — 10μa 1000 KΩ — 1μa 10,000 KΩ — 100 na
Resolution:	0.001% of Range in 5-1/2 digit mode (1 milliohm in .1 KΩ Range). 0.01% of Range in 4-1/2 digit mode (10 milliohms in .1 KΩ Range).
Accuracy, Short Term, 5-1/2 Digit Mode (after DIGITAL ZERO Command):	24 hrs., 23°C ± 1°C ± (0.03% Rdg + 5 digits).
Accuracy, 6 months, 23°C ± 5°C, 5-1/2 Digit Mode (after DIGITAL ZERO Command):	± (0.1% Rdg + 10 digits).
Temperature Coefficient, 5-1/2 Digit Mode (after DIGITAL ZERO Command at new Temperature):	.1 KΩ - 1000 KΩ Ranges: ± (0.01% Rdg + 2 digits)/°C. 10,000 KΩ Range: ± (0.015% Rdg + 2 digits)/°C.
Voltage Protection: (without damage)	± 375 VDC or peak AC.
Settling Time: (Unfiltered)	0.1 KΩ - 100 KΩ Range: 30 ms to within 10 digits of final value. 1000 KΩ Range: 40 ms to within 10 digits of final value. 10,000 KΩ Range: 300 ms to within 10 digits of final value.
Settling Time: (Filtered)	500 ms to within 10 digits of final value.

Table 1.2 - Specifications continued

MODEL 5005 AVERAGING AC/DC CONVERTER	
Ranges	4 Ranges, 1 through 1000V
Resolution	.001% F.S. in 5½ Digit Mode .01% F.S. in 4½ Digit Mode
Maximum Input Voltages	1000V RMS from 30 Hz to 20 KHz decreasing linearly to 20V RMS at 1 MHz. Maximum input voltage on any range: $<2x10^7$ Volt-Hz
Accuracy 6 months: 23°C ± 5°C **(All Ranges included except: 1000V Range from 100 KHz to 250 KHz Range)** **For inputs greater than 500V, add .1% of reading to above**	30 Hz to 50 Hz: ± .2% of rdg ± .02% of F. S. (Filtered) 50 Hz to 30 KHz: ± 0.1% of reading ± .02% of F. S. 30 KHz to 100 KHz: ± .15% of reading ± .02 of F. S. 100 KHz to 250 KHz 1V, 10V, 100V Ranges: ± 1% of rdg ± .1% of F. S. 1 KV Range: Not applicable 250 kHz to 1 MHz ± (20% R + 4% F. S.)
Overload Recovery	1.5 seconds maximum to .1% of F.S. from 1000V overload. 600 ms maximum to .1% of F.S. from 100% overload. (4 times full scale)
Settling Time	400 msec maximum to settle to .1% of F. S.
Common Mode	>80 dB at 60 Hz with 100Ω unbalance in either lead.
Input Impedance	1 MΩ ± 0.1% in series with .22 μF, shunted by less than 200 pF to common.
Temperature Coefficient	30 Hz to 30 KHz: (+ .01% rdg + .002% F.S.) /°C 30 KHz to 250 KHz: (± .05% rdg ± .005% F. S.)°C

MODEL 5006 TRUE RMS AC/DC CONVERTER	
Ranges	4 Ranges: 1V to 1KV
Resolution	.001% of Range in 5½ Digit Mode .01% of Range in 4½ Digit Mode
Maximum Input Voltage	1000V DC/RMS or 1500V peak, decreasing to 20V RMS at 1 MHz. $2 x 10^7$ V Hz max in any range
Settling Time: Zero to Full Scale	Settles to within .01% of range. 400 msec
Input Impedance Front Input	1 MΩ ± .1% in series with .22 μF, shunted by less than 200 pF to common. In DC mode the .22 μF Capacitor is shorted.
Common Mode Rejection with 100 Ω unbalance in either lead. DC and 60 Hz	80 dB
Accuracy, Short Term **AC coupled** **Sine Wave Input .1% F.S.≤ V_{IN} ≤200% F.S.** **For V_{IN}≥500V add .1% of reading to above.** **Frequency xV_{IN} ≤$2x10^7$V-Hz** **≤75% R. H.** **For DC coupled, add .02% F.S. to AC specs.**	(24 Hrs., 25°C + 1°C) 20 Hz - 30 Hz: (Filtered) ± (0.5% R + .03% F. S.) 30 Hz - 50 Hz: (Filtered) ± (.25% R + .03% F. S.) 50 Hz - 20 KHz: ± (.09% R + .03% F. S.) 20 KHz - 50 KHz: ± (.09% R + .09% F. S.) 50 KHz - 100 KHz: ± (.38% R + .18% F. S.) 100 KHz - 300 KHz: 10,100V Range ± (3% R + .5% F. S.) 1V Range: ± (5% R + 1% F. S.) 300 kHZ - 1 MHz: ± (23% R + 5% F. S.)

Table 1.2 - Specifications continued

TRUE RMS AC (5006) continued	
Accuracy, Long Term, AC Coupled, Sine Wave Input .1% F. S. ≤ V_{IN} ≤ 200% F. S. For V_{IN} > 500V, add .1% of reading to above Frequence x V_{IN} ≤ $2x10^7$ V-Hz ≤ 75% R. H. for DC coupled, add .02% F. S. to AC specs	(6 Months, 25°C ± 5°C) 20 Hz - 50 Hz (Filtered): Same as 24 hour spec. ± .03% F. S. 50 Hz - 20 KHz: Same as 24 hour spec. ± (.03% R ± .03% F. S.) 20 KHz - 50 KHz: Same as 24 hour spec. ± (.05% R ± .04% F. S.) 50 KHz - 100 KHz: ± (.6% R ± .3% F. S.) 100 KHz - 300 KHz 10,100V Range: ± (4% R ± 1% F.S.) 1V Range: ± (6% R ± 2% F.S.) 300 KHz - 1 MHz: ± (24% R + 6% F. S.)
Temperature Coefficients 0°C to 50°C AC coupled (to 20 KHz) 1, 10, 100, 1000V Ranges DC coupled (to 20 KHz) 1, 10, 100, 1000V Ranges	 ± (.005% R + .003% F. S.) / °C ± (.005% R + .005% F. S.) / °C
Crest Factor	7:1 at Full Scale $7 \times \sqrt{\frac{F.S.}{V_{IN}}}$ for other voltages

4-1/2 DIGIT MODE	
Functions and Ranges:	All Functions and Ranges.
Selection:	May be selected via front panel keyboard (RESOL Key) or GPIB command.
Display:	4 full decades plus overrange digit.
Read Rate: (Internal Trigger): (External or GPIB Trigger):	40 readings/sec (60 Hz instrument) 33 readings/sec (50 Hz instrument) 20 readings/sec (60 Hz instrument) 18 readings/sec (50 Hz instrument)
Accuracy (same conditions as 5-1/2 digit mode):	"X" % Rdg + "Y" digits where: "X" is the percentage error specified for 5-1/2 digit operation, or ± .01%, whichever is greater. "Y" is equal to the number of digits specified for 5-1/2 digit operation divided by 10, or ± 5 digits, whichever is greater.
Normal Mode Rejection Ratio:	Same as for 5-1/2 digit operation.

EXTERNAL REFERENCE (SOFTWARE RATIO)	
Available Functions	DC/DC, AC/DC, Ohms/DC DC/AC, AC/AC, Ohms/AC
Available Ranges	All ranges normally available, including AUTORANGE
Maximum Input Voltage	± 400 V maximum instantaneous voltage between SIGNAL and REFERENCE input terminals
Accuracy	± [(Signal Accuracy) + (Reference Accuracy) • (RR/RI* or 1.0, whichever is greater)]

*RR = Reference Range
RI = Reference Input

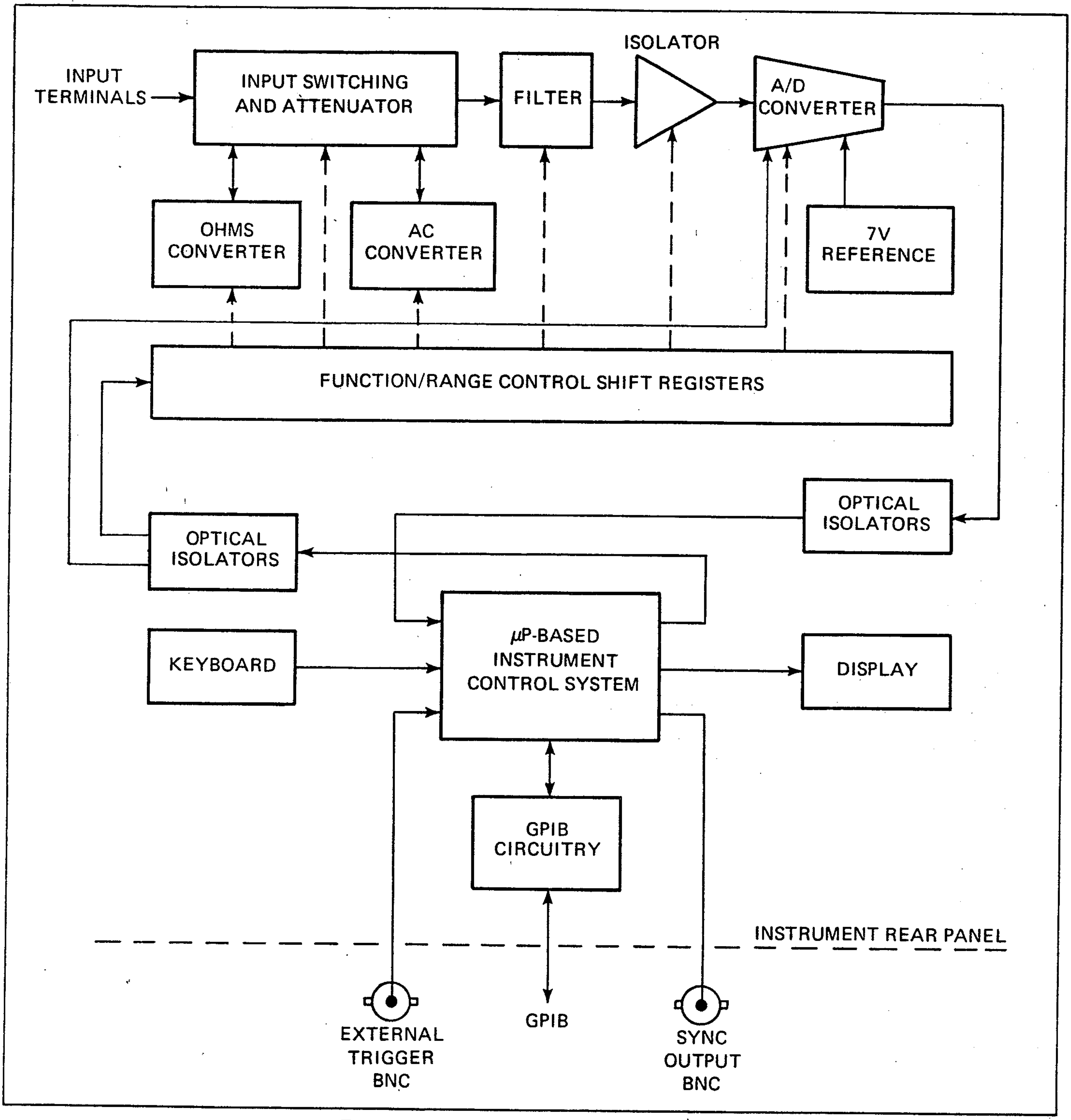


Figure 1.1 - Model 5005/5006 DMM Block Diagram

120, 220, and 240 VAC ± 10%, 47 to 440 Hz. The installation, section 2 presents the AC line cord requirements, and the AC primary voltage selection instructions.

1.7 SPECIFICATIONS.

1.7.1 The published specifications for the Racal-Dana Model 5005/5006 are listed in Table 1.2. These specifications establish the validation for the calibration and speci fication checks listed in this manual.

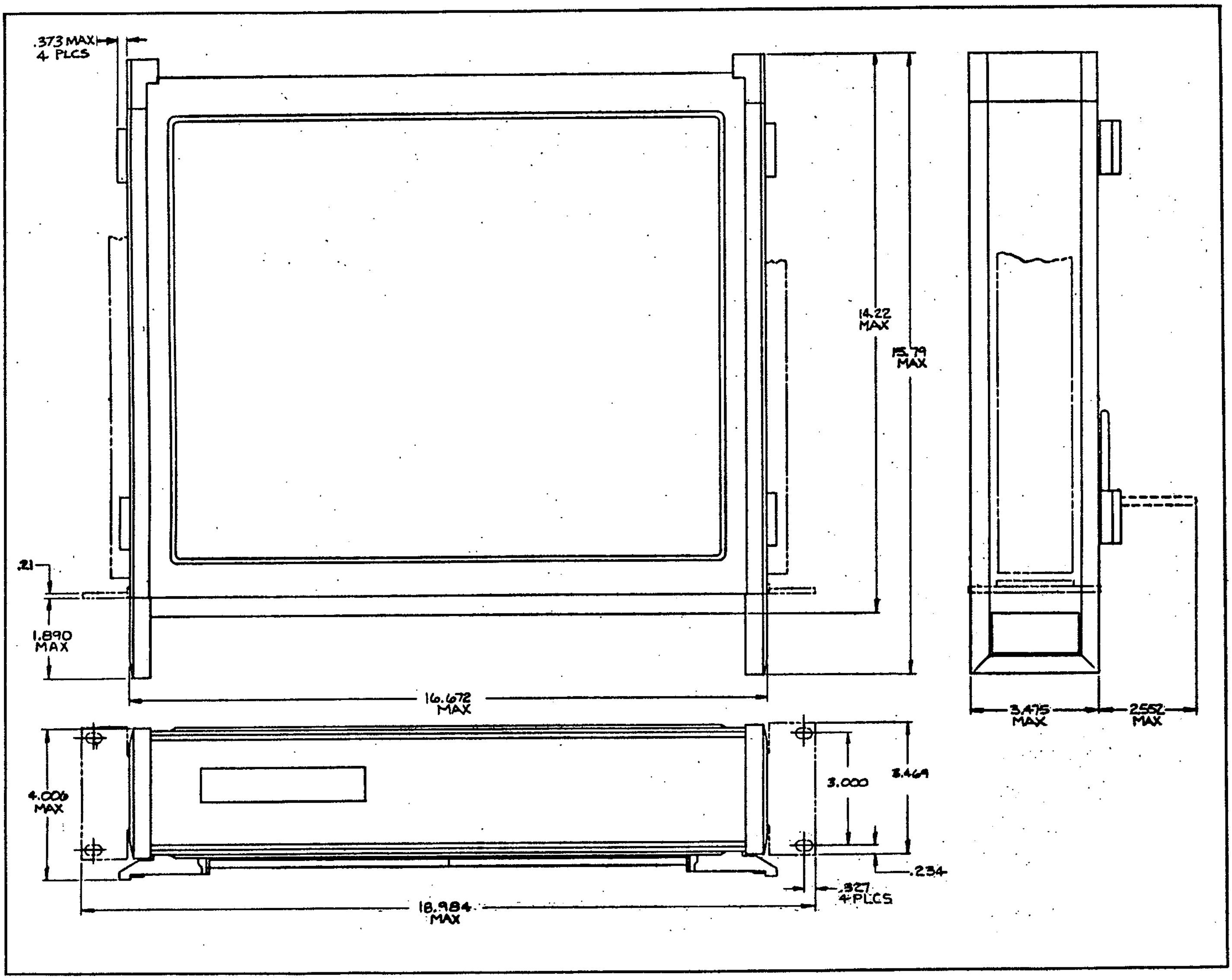


Figure 1.2 - Dimensional Outline

2.1 PURPOSE

2.1.1 This section describes the instrument installation for bench or rack mounting and optional package installation as may be required.

2.2 DMM UNPACKING AND INSPECTION.

2.2.1 The instrument's carton and plastic-foam packaging meets the impact and drop requirements of the NSTC Test Procedures 1 and 1A. This precaution eliminates most shipping problems.

2.2.2 Prior to unpacking the instrument, examine the exterior of the shipping carton for any signs of damage (all irregularities should be noted on the shipping bill). Carefully remove the instrument from the carton's plastic-foam packaging and inspect the instrument for any signs of damage. Notify the carrier immediately if damage is apparent and a qualified personnel should check the unit for safety.

2.3 BENCH OPERATION.

2.3.1 Each instrument is equipped with a tilt ball or "kickstand" to elevate the front of the instrument for easy operation. The tilt ball is attached to the two forward feet at the bottom of the instrument. When used, the ball is pulled down to its vertical position.

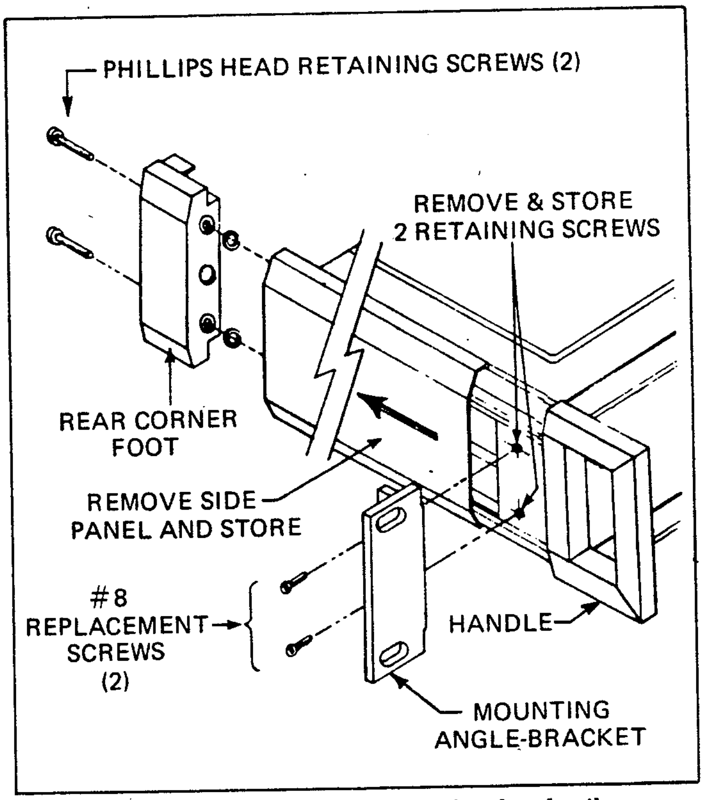


Figure 2.1 - Fixed-mount angle-bracket detail

2.4 EQUIPMENT-RACK INSTALLATION.

2.4.1 General.

2.4.1.1 The instrument can be mounted in a standard 19 inch equipment-rack with an optional "FIXED-MOUNT" installation package or an optional "SLIDE-MOUNT" installation package. The instructions for each installation are described in subsections 2.4.2 and 2.4.3, listed next.

2.4.2 Fixed-Mount Installation. Option 60.

2.4.2.1 The fixed-mount installation package includes a pair of handle-sub corner inserts for the non-handle installation, a pair of custom mount angle-brackets and 4 flat head 8-32 x 5/16 screws. To install the angle-brackets, refer to Figure 2.1 for an illustrated example then proceed as follows.

2.4.2.2 To remove the bench feet, bail, or top and bottom covers, unscrew the two phillips-head retaining screws from the corner-feet about 3/4 inch. To slide off the side panels remove the retaining screws and corner feet completely.

2.4.2.3 Next, slide the cover 1/2 inch towards the rear panel then lift off. Remove the four bench-feet from the bottom cover by unscrewing the phillips-head retaining screw from each foot.

2.4.2.4 Remove the side panels by sliding them down the retaining track in the direction of the rear corner-feet. With the side panels off, the handle brackets retaining screws are exposed. Store the panels wherever convenient.

2.4.2.5 The two retaining screws in each handle are removed but either the handle or the handle-sub corner insert must remain in the handle position.

2.4.2.6 The angle-bracket is placed over the handle or handle-sub with the screw holes aligned over the handle holes. Insert the 2 flat-head #8-32 x 5/16 screws through both the angle-bracket and handle, then screw to the frame.

2.4.2.7 Re-install the feet at each corner of the cabinet to complete the installation.

2.4.3 Slide-Mount Installation. Option 67.

2.4.3.1 The slide-mount installation package includes the following hardware:

a. 2 custom-mount angle-brackets
b. 6 alignment blocks
c. 2 front slide-mount brackets
d. 2 rear slide-mount brackets
e. 2-triple-rail slide-mount assemblies
f. 12 self-anchoring #10-32 tinnerman nuts
g. 8 Phillips pan-head screws#10-32 x 1/2
h. 6 slotted #8-32 x 3/8 pan-head screws with nuts, washers, and lock washers.
i. 8 phillips pan-head, self-tapping screws #8-32 x 5/16
j. 4 phillips flat-head, self-tapping screws #8-32 x 5/16
k. 4 phillips pan-head screws #10-32 x 3/4
l. 2 alignment spacers (washers) #8 x 1/16
m. 2 handle-sub corner inserts

2.4.3.2 To install the Alignment Blocks in the channels along each side of the instrument, remove the side panels from the instrument by first removing two corner-feet by extracting the two phillips-head retaining screws. This detail is shown in Figures 2.1 and 2.2.

2.4.3.3 Next slide the covers 1/2 inch toward the rear panel then lift off. Remove the four bench-feet from the bottom cover.

2.4.3.4 Remove the side panels by sliding them down the retaining track in the direction of the rear corner-feet. With the side panels off, the handle brackets retaining screws are exposed. Store the panels wherever convenient.

2.4.3.5 The 2 handle-retaining screws are removed from each handle. This permits the handles to slip freely from the instrument.

2.4.3.6 Slide 3 alignment-blocks down each channel which are exposed by the removed handles. The drawing in Fig. 2.2 presents the front-left corner of the instrument with the handle removed. The alignment-blocks will move freely along the length of the channel on each side of the instrument.

2.4.3.7 Next, the handles, or the handle-subs, are returned to the original handle position and the custom-mount angle bracket is placed over the handle with the screw holes

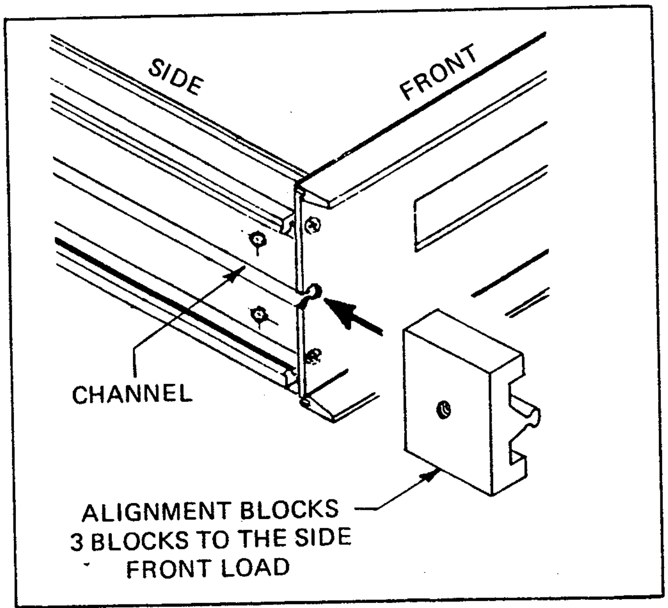


Figure 2.2 - Loading the alignment blocks

aligned over the handle holes. Insert 2 phillips flat-head 8-32 x 5/16 screws through both the angle-bracket and the handle, then secure to the frame. The installation of the custom mount angle-bracket completes the instrument preparation.

2.4.3.8 The following paragraph describes the preparation of the triple-rail slide-mount assembly for installation inside the equipment rack. The hole alignment on the slide-mount is an important consideration during installation, therefore physically extend and retract the slide-mount. An extended view of the slide-mount with the rear mounting bracket attached is shown in Fig. 2.3. As the slide-mount is extended and retracted, it should be noted that all holes on the instrument-rail and the rack-rail are accessible either directly or through the enlarged holes in the center-rail.

2.4.3.9 Preparing the triple-rail slide-mount for rack installation requires the following assembly:

a. Place the front slide-mount bracket, (with one mounting slot) with nut-fastening slots down, on the bench.

b. Position the front end (slide-out end) of the slide-mount over and parallel to the bracket, with the rack-rail resting within the bracket, approximately 3/4 inch from the front edge of the bracket.

c. Adjust the rails to align the rack-rail and the front-bracket holes, then place a slotted pan-head #8-32 x 3/8 screw through the holes. Attach the matching washer, lock-washer and nut to the screw and secure firmly, while maintaining the 3/4 inch dimension to the front of the bracket. Refer to Fig. 2.3 for illustrations that detail the slide-mount and bracket assembly.

d. Position the rear bracket on the opposite end of the slide-mount in the same manner as the front bracket. Adjust the rails to align the holes and place two #8-32- 3/8 screws through the holes securing the slide-mount loosely to the rear bracket with washers, lock-washer and nut.

e. Slide two self-anchoring #10-32 tinnerman nuts onto each front and rear mounting-bracket nut-fastening slots.

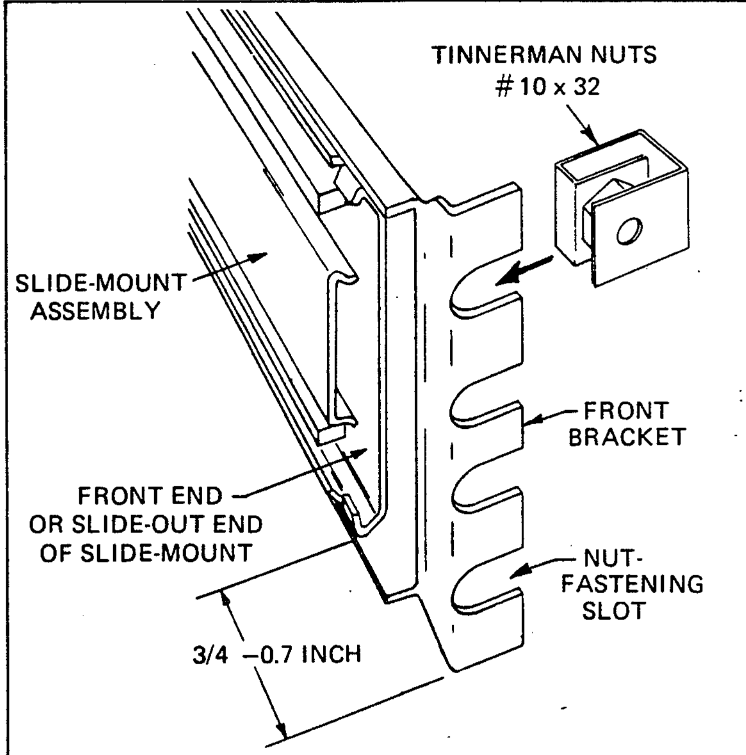
f. Complete the second slide-mount and bracket assembly in the same manner.

2.4.3.10 The following equipment-rack assembly instructions may require the assistance of another person. The slide-mount assembly is positioned in the designated area of the equipment rack and the installation sequence follows: NOTE: If the rack flange is tapped for #10-32 screws, drill out with a 1/4 inch diameter drill bit two places for each bracket.

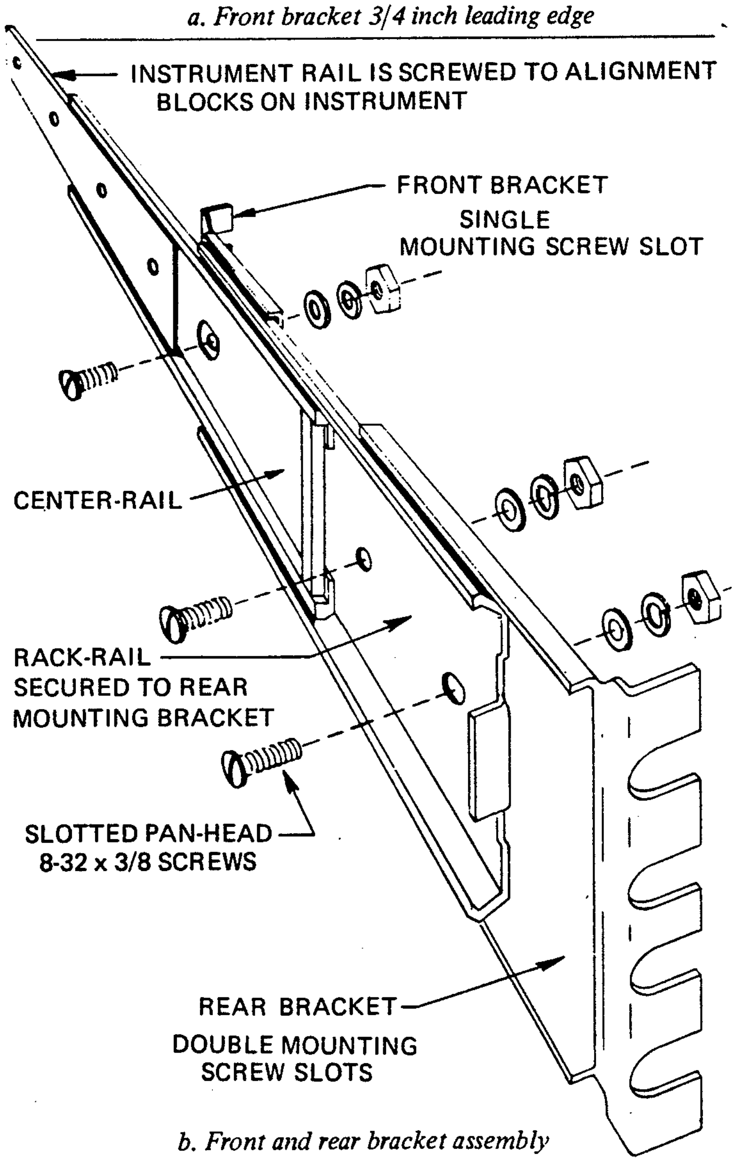
a. Hold the front bracketted-end (with tinnerman nuts) of the slide-mount behind the rack flange, while the second person holds the rear-bracket end.

b. Secure the front bracket to the rack flange with two #10-32 x 1/2 screws. Seat the bracket firmly against the rack flange before tightening the screws.

c. Install the second bracket-slide-mount assembly on the rack in the same manner as the first, then set the front dimension between the slide-mounts at 16-5/8 inches.



a. Front bracket 3/4 inch leading edge



b. Front and rear bracket assembly

Figure 2.3 - Slide-mount and bracket assembly

d. Extend the length of the rear mounting bracket until the bracket seats behind the rack flange. Tighten the rear-bracket assembly screws.

e. The distance between the slide-mounts at the rear bracket position must be 16-5/8 inches. If a filler-plate is required to secure the slide-mount at 16-5/8 inches employ the dimensions supplied in Fig. 2.4 for calculations.

f. Secure the rear bracket (with tinnerman nuts) to the rack flange (or filler-plate) with two #10-32 x 1/2 screws in each bracket.

g. The triple-rail slide-mounts should move freely to the maximum extended position If not, clear any obstacle before installing the instrument.

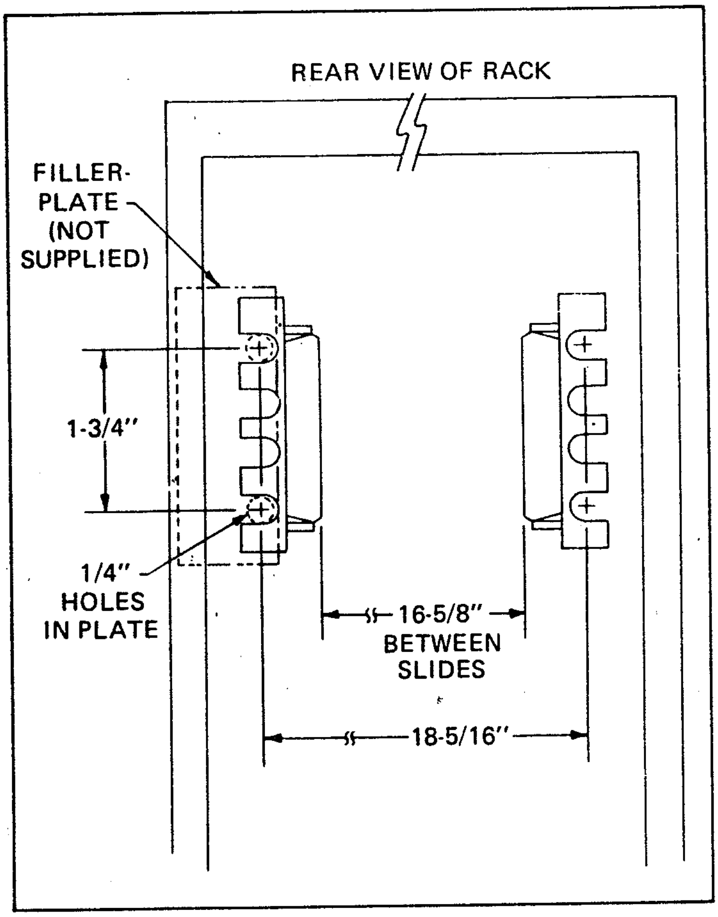


Figure 2.4 - Rear end slide-mount rack dimensions

2.4.3.11 The following procedure which describes the instrument installation to the side-mount implies that another person will assist.

a. Pull the rails to the maximum extended length. Insert a #8-32 x 5/16 Phillips pan-head self-tapping screw inward through the first mounting hole in each instrument rail. On the other side of the instrument rail, place an alignment spacer on the same screw.

b. Position the instrument between rails so that first screw-hole immediately behind the handle on each side, line up with the screws held by the rails. Keeping the alignment spacer between the rail and instrument seat the self-tapping screws to a pull-up position. The unit and slide-mount assembly are illustrated in Fig. 2.5.

c. Using the first mounting screw as a pivot, align the instrument with the rails and slide the front alignment-block behind the second hole on the rail. When hole alignment is obtained, screw in another #8-32 x 5/16 self-tapping screw.

d. Repeat this procedure for the remaining alignment-blocks. It is necessary to slide the rails to and fro until an access hole is located in the center-rail which aligns the instrument rail hole with the alignment-block hole.

e. Firmly seat all the self-tapping screws through the instrument rails. The instrument should slide freely on the rail.

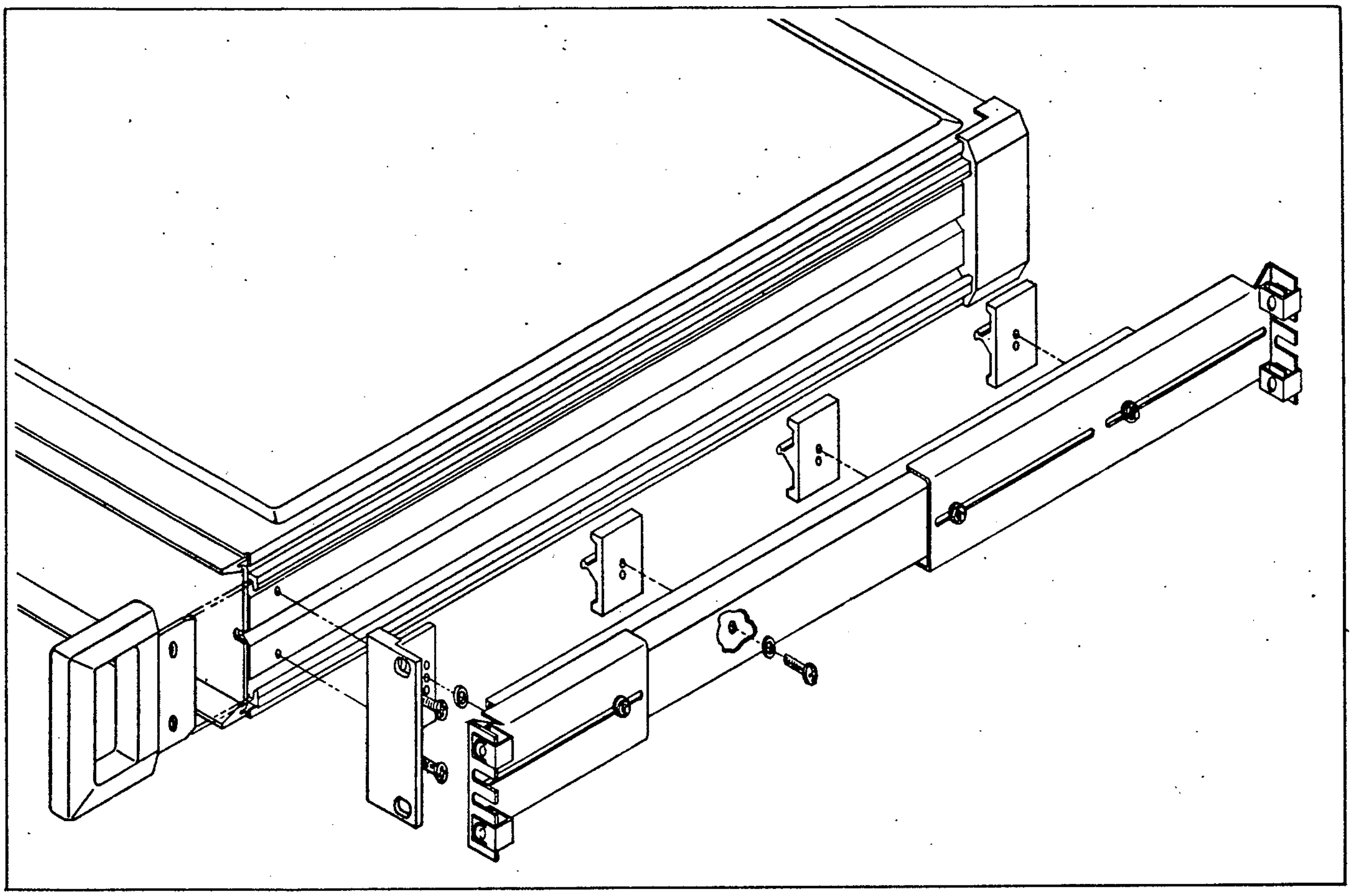


Figure 2.5 - Slide-mount and Instrument Assembly

2.4.3.12 Locking the instrument into the normal operating position on the rack requires the following assembly:

a. Slide two #10-32 self-anchoring tinnerman nuts on the rack flange (each side) inline with the slots in the angle-bracket. If the rack-flange is tapped for #10-32 screws, omit the tinnerman nuts.

b. Slide the instrument fully into the rack until the angle-bracket strikes the slide-mount bracket screws. Secure in place with 4 Phillips pan-head #10-32 x 3/4 screws. The installation is complete.

2.5 AC POWER CONNECTIONS.

2.5.1 Standard units operate on either 100, 120, 220 or 240 volts, 60 Hz (50 to 400 Hz available). Power consumption is less than 25 watts. Operation on any one of the four line voltages is selected by the placement of a small printed circuit card (P2), located in J2 receptacle on the main PCB. Selection of a specific line voltage is accomplished as follows:

2.5.1.1 Disconnect the power cord from the AC power source.

> **WARNING**
>
> Removal of covers exposes potentially lethal voltages. Avoid contact with internal electrical connections while unit is connected to AC power source.

2.5.1.2 Remove the instrument top cover by removing each corner foot as described in paragraph 2.4.2.2. Next, slide the top cover toward the rear panel approximately half inch, then lift the cover from the frame.

2.5.1.3 Remove the two screws holding the plastic protective cover over the voltage selector.

2.5.1.4 Remove the voltage card-selector P2 from the J2 receptacle, then reinsert it permitting the desired line voltage number to be visible through the small view window on the rear panel of the instrument.

2.5.1.5 To reassemble the instrument, place the top cover on the frame with the side flanges fitting correctly in the frame grooves and the front edge of the cover approximately one inch from the front panel. When correctly seated on the frame, slide the cover forward until the front edge slides under the front panel. Replace the rear corner feet, insuring that the top cover rear corners slide under the paw on each rear foot.

2.6 GROUNDING REQUIREMENTS.

2.6.1 The front panel and cabinet of the instrument are grounded in accordance with MIL-T-28800B to protect the user from possible injury due to shorted circuits. The three conductor AC power cable (P/N 600620) supplied with the instrument maintains a low impedance path to ground when connected to a three wire single phase AC receptacle. This device or other devices connected to or in proximity to this instrument must maintain the third-wire earth ground intact as stated in current regulations.

2.7 SHIPPING CONTAINER REQUIREMENTS.

2.7.1 When shipping the instrument, the original shipping carton with the plastic packaging forms and plastic dust cover provide the necessary protection during trans-shipments. This carton should be preserved if possible.

2.7.2 When the original shipping carton is not available, reconstruct the packaging using a can of spray plastic foam to surround the plastic-wrapped unit in the carton.

2.8 INPUT-OUTPUT CABLES.

2.8.1 The input terminals used on the front and rear panels are standard banana jacks. The spacing among the banana jacks permits a molded dual banana plug to be connected directly between binding posts. The dual banana plug cables are available under Racal-Dana part number 402190.

2.8.2 The BNC connectors mounted on the rear panel are standard items common to systems installations, therefore not supplied by Racal-Dana.

2.8.3 The interface connector, common to IEEE-488-78 and Racal-Dana's GPIB; mounted on the rear panel accepts the standard IEEE-488 connector, Racal-Dana's part number 406845, GPIB cable, 1 meter (3.28 ft.): 406844, GPIB cable, 2 meters (6.56 ft.); 406846, GPIB cable, 4 meters (13.12 ft.).

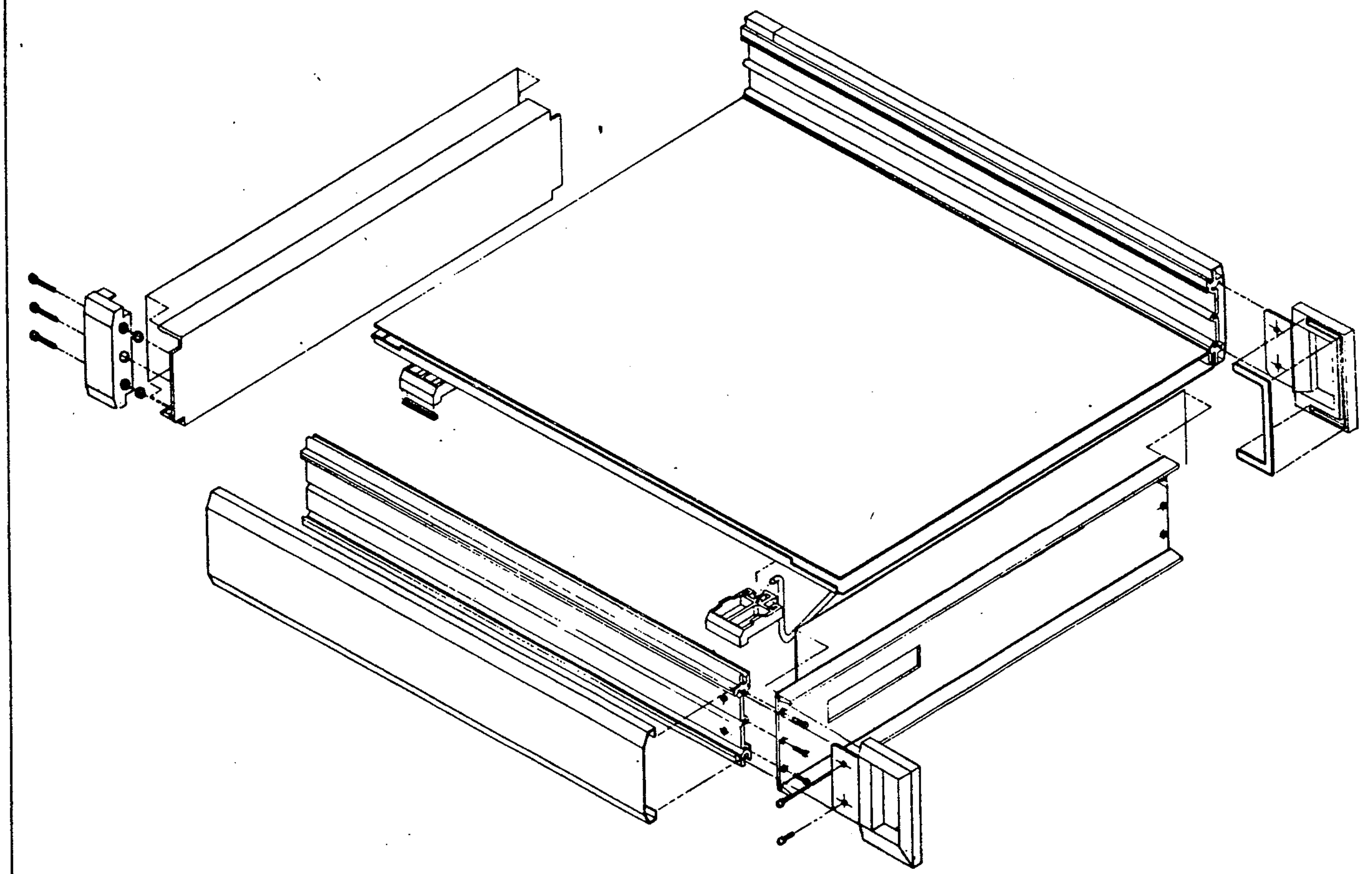


Figure 2.6 - Cabinet Exploded View

3.1 INTRODUCTION.

3.1.1 This section contains operating information for the DMM. The information contains illustrations of all front and rear panel controls, indicators and connectors along with tabular listing of the function and purpose for each. Operating instructions for manual or bench operation are presented in two ways; a description of each operating feature followed where necessary, with a step-by-step operating example. Some operating features or functions are simple one or two step operations and thus no operating examples are included.

3.1.2 Remote operation via the IEEE-STD-488-1978 General Purpose Interface Bus is one of the principal features of the DMM. This section presents bus address selection information and a tabular listing of the device-dependent messages used to program the instrument. Also included is a GPIB program, measurement and data transfer example.

3.2 OPERATION.

3.2.1 Before operating the instrument, it is strongly recommended that the operator read this entire section in order to avoid damage to the unit. After reading the operating instructions, refer to the installation section, then check the position of the line voltage selector through the viewing window on the rear panel.

CAUTION

This instrument may be damaged if operated on line voltage other than that called for by the line voltage selection card, P2.

WARNING

Removal of covers exposes potentially lethal voltages. Avoid contact with internal electrical connections while unit is connected to AC power source.

3.2.2 After ensuring that the line voltage selector is in the proper position and the cover on the instrument replaced, connect the power cord to the AC outlet and depress the POWER switch to power-up to DMM. The DMM will display 5005 or 5006 upon applying power and the LED annunciators and AUTO are ON.

3.3 CONTROLS AND INDICATORS.

3.3.1 The front panel keyboard switches execute all the functions and modes of operation when the DMM local function is selected.

3.3.2 The panel designators, keyboard switches (refer to as key) and locations for all controls, indicators, and connectors are illustrated on Figure 3.1 and Figure 3.2. The description for each are itemized in Table 3.1 and Table 3.2.

3.4 BASIC MEASUREMENTS.

3.4.1 Digital Zero Command.

3.4.1.1 This procedure should be employed after turn-on and at other selected intervals to verify the DMM's zero accuracy in the DC function.

3.4.1.2 To check the DMM's zero accuracy, short the HI-LO INPUT terminals together and verify a display read-out of zero ± 3 digits in each DC range. If the reading exceeds this limit in any range, perform a digital zero command as described below:

a) Short the HI-LO INPUT terminals.

b) Select the DC function, .1 range.

c) Depress and hold the .1 Range Key until the display reads "CAL 0", verifying that the zero command was enabled. Release the .1 range key.

d) REMOTE OPERATION: The GPIB command K2, the digital zero command program instruction is described in paragraph 3.5.18.

3.4.2 Range Control.

3.4.2.1 Upon initialization, the DMM goes to its home state; autorange and continuous readings. With a signal applied to the input HI-LO terminals, the autorange will set the range to match whatever signal the DMM sees at the input terminals. For example, if a 6 volt battery is connected to the input terminals and the DMM is initialized by power turn-on, the DMM goes through the auto-test routine and the autorange will select the 10 volt range.

3.4.2.2 To manually disable autorange, depress one of the range keys. This action extinguishes the autorange annunciator and the DMM will now respond to the selected range.

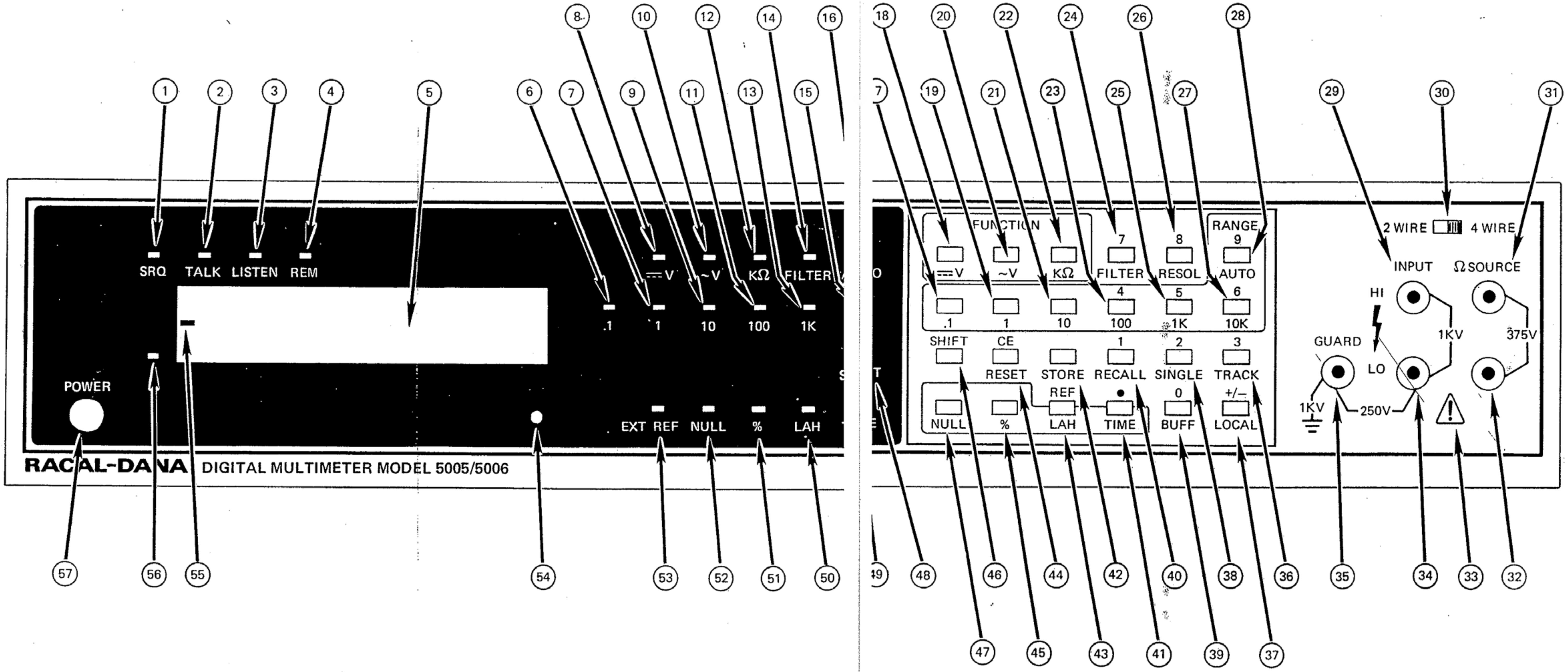


Figure 3.1 - Front Panel Location Guide

Table 3.1 - Front Panel Controls, Connectors and LEDs

Reference	Designator/Label	Functions
(1)	SRQ LED ANNUNCIATOR	ON: Indicates that the DMM is transmitting a service request (interrupt) to the controller in systems operation.
(2)	TALK LED ANNUNCIATOR	ON: Indicates that the DMM is programmed by the controller to function as a talker on the GPIB.
(3)	LISTEN LED ANNUNCIATOR	ON: Indicates that the DMM is programmed by the controller to function as a listener on the GPIB.
(4)	REM LED ANNUNCIATOR	ON: Indicates that the controller has placed the instrument in the remote operation mode.
(5)	DISPLAY LEDs 7-SEGMENT	These LEDs display the value of the input signal with appropriate decimal point. They are also used to display constants and function symbols.
(6) ↓ (16)	MATCHING DESIGNATORS ANNUNCIATOR LEDs	This group of designators match the designators for Function, Range, Filter and Auto-Ranging. The illuminated LED agrees with the key selected.
(17)	□ .1 RANGE SELECTOR KEY	Selects .1 VDC or .1 KΩ ranges. ".1" annunciators illuminate.
(18)	□ ⎓V FUNCTION SELECTOR KEY	Selects DC Function, enables autoranging and continuous readings (internal trigger). ⎓V annunciator is illuminated.
(19)	□ 1 RANGE SELECTOR KEY	Selects 1 VDC, 1 VAC or 1 KΩ ranges. "1" annunciator is illuminated.
(20)	□ ~V FUNCTION SELECTOR KEY	Selects True RMS AC Function, enables autoranging and continuous readings (internal trigger). ~ V annunciator is illuminated.
(21)	□ 10 RANGE SELECTOR KEY	Selects 10 VDC, 10 VAC or 10 KΩ ranges. "10" annunciator is illuminated.
(22)	□ KΩ FUNCTION SELECTOR KEY	Selects Resistance Function, enables auto-ranging and continuous readings (internal trigger). KΩ annunciator is illuminated.
(23)	□ 100 RANGE SELECTOR KEY	Selects 100 VDC, 100 VAC or 100 KΩ ranges. "100" annunciator is illuminated.
(24)	□ FILTER FILTER SELECTOR KEY	Toggles the 3-pole active filter. FILTER annunciator is illuminated when filter is selected.
(25)	□ 1K RANGE SELECTOR KEY	Selects 1 KVDC, 1 KVAC or 1000 KΩ ranges. "1K" annunciator is illuminated.
(26)	□ RESOL RESOLUTION SELECTOR KEY	Selects 4-1/2 digit mode if operating in 5-1/2 digit mode; selects 5-1/2 digit mode if in 4-1/2 digit mode.

Table 3.1 - Front Panel Controls, Connectors and LEDs continued

Reference	Designator/Label	Functions
(27)	□ 10K — RANGE SELECTOR KEY	Selects 10,000 KΩ range. "10K" annunciator is illuminated.
		NOTE: Selection of any range key disables auto-ranging.
(28)	AUTO — AUTO-RANGING SELECTOR KEY	Toggles AUTO ranging mode. If AUTO ranging is selected, depressing this key or a range key returns to manual range control. AUTO annunciator is illuminated when in auto-ranging mode.
(29)	HI INPUT BANANA JACK	+ Signal Input (J104).
(30)	2-WIRE/4-WIRE SWITCH	Front panel mounted slide switch that connects Ω SOURCE terminals to INPUT terminals for two wire resistance measurements when in 2-wire position. Terminals are disconnected in 4-wire position.
(31)	Ω SOURCE BANANA JACK	Ω CURRENT RETURN (J105).
(32)	Ω SOURCE BANANA JACK	Ω CURRENT SOURCE (J103).
(33)	⚠ CAUTION SYMBOL	REFER TO THE MANUAL IN ORDER TO PROTECT THE INSTRUMENT AGAINST DAMAGE.
(34)	LO INPUT BANANA JACK	– Signal Input (J102).
(35)	GUARD BANANA JACK	Front Panel connector to internal guard shield (J101).
(36)	□ TRACK — READ-OUT SELECTOR KEY	Causes instrument to take continuous readings at maximum read rate (internal trigger).
(37)	□ LOCAL — LOCAL SELECTOR KEY	Returns control from GPIB to front panel (if not disabled from controller). Displays instrument's GPIB address while Key is held depressed.
(38)	□ SINGLE — READ-OUT SELECTOR KEY	Causes instrument to go into "Hold" mode. Takes single reading each time Key is depressed.
(39)	□ BUFF — DATA BUFFER SELECTOR KEY	Provides a means for recalling previous readings from the data buffer to the display. Pressing the button for more than 5 seconds will clear the data buffer.
(40)	□ RECALL — RECALL SELECTOR KEY	Enables RECALL access for the constants previously stored as Null, %, LAH, and BUFF.
(41)	□ TIME — TIME SELECTOR KEY	Provides a means of taking a series of measurements under control of the voltmeters built-in real-time clock. Start time, stop time and reading intervals can be selected and entered via the keyboard. TIME annunciator is illuminated when instrument is under control of Time function.

Table 3.1 - Front Panel Controls, Connectors and LEDs continued

Reference	Designator/Label	Functions
(42)	☐ STORE — STORE ENABLER KEY	Stores number on display, last reading or numerical entry.
(43)	☐ LAH — LOW-AVERAGE-HIGH FUNCTION SELECTOR KEY	Selects function that compares the present reading with previously determined Low (most negative) or High (most positive) readings. Stores the present reading in place of one of these if it is found to be lower or higher. Also calculates and stores the average value of a selected number of readings. The Low, Average, High or number of readings averaged can be selected for a continuous display or recalled from memory and displayed. The number of readings to be averaged can be entered prior to selection of LAH operation, and this number can be recalled from memory and displayed. LAH annunciator is illuminated when function is enabled.
(44)	☐ RESET — RESET KEY	Removes previously selected "Math" functions. Enables continuous readings and lights all front panel annunciators and display segments.
(45)	☐ % — PERCENT FUNCTION SELECTOR KEY	Calculates and displays: $\frac{\text{Reading-Percent Constant}}{\text{Percent Constant}} \times 100$ which is the percentage deviation of the input reading from a reference value called "Percent Constant" (stored reading or constant entered via keyboard). % annunciator is illuminated when % function is enabled.
(46)	☐ SHIFT — TOGGLE KEY	Allows access to numeral entry, Ext. Ref and Clear Entry keys. SHIFT annunciator indicates whether the keyboard is in the shifted or unshifted mode.
(47)	☐ NULL — NULL FUNCTION SELECTOR KEY	Selects Null function. When selected, the number on the display is stored as a Null constant and is subtracted from all future readings until the Null function is disabled by depressing the NULL key again. The Null constant can be either the measurement value at the time Null is selected or a value entered via the keyboard. NULL annunciator is illuminated when Null function is enabled.

Table 3.1 - Front Panel Controls, Connectors and LEDs continued

Reference	Designator/Label	Functions
	DOUBLE KEY-STROKE ENTRY The following keys are SHIFT functions	
	□ SHIFT CE □	The "Clear Entry" key clears numbers entered into display and returns the instrument to its previous state.
	□ SHIFT N □	Where N = 0 to 9. Enters numbers into display in preparation for storage in memory as constants (e.g., Null Constant, Reference Value for percent deviation, etc.). Depressing these keys does not unshift keyboard.
	□ SHIFT □ +/–	Reverses sign (polarity) of number entered into display. Depressing this key does not unshift keyboard.
	□ SHIFT □ REF	Enables and disables the external reference selection mode. When enabled,"REF" is displayed on the front panel read-out. Refer to Section 3.4 for complete procedure.
	□ STORE □ NULL	Stores number on display (last reading or numerical entry) as Null Constant.
	□ STORE □ %	Stores number on display (last reading or numerical entry) as Percent Constant for percent deviation calculation.
	□ STORE □ LAH	Stores numerical entry on display as number of readings to be averaged (c).
	□ STORE □ TIME X □	Stores numeral entry on display as parameter associated. with Time function, where X is: 1. START Time 2. STOP Time 3. Time INTERVAL 4. Time SUBINTERVAL 5. N (number of readings per INTERVAL) 6. PRESENT Time
	□ STORE SHIFT □ N □	Where N = 0 to 9. Stores the present instrument setting into the buffer program location 0 to 9.
	□ RECALL □ %	Displays Reference Value used in percent calculations.
	□ RECALL □ LAH	Recalls Low (L), Average of last N readings (A), High (H), number of readings that have been averaged (n), and the number of readings to be averaged (c). The number of readings to be averaged (c) is entered via the keyboard prior to selecting LAH operation. c = 4 if no entry is made.

Table 3.1 - Front Panel Controls, Connectors and LEDs continued

Reference	Designator/Label	Functions
	☐ RECALL ☐ BUFF	Recalls readings stored in buffer memory to the display.
	☐ RECALL ☐ NULL	Displays value of Null constant.
	☐ RECALL SHIFT ☐ N ☐	Where N = 0 to 9. Recalls machine settings previously stored in program buffer and programs the instrument to these settings.
(48) ↓ (53)	MATCHING DESIGNATORS ANNUNCIATOR LEDS	This group of annunciator LEDs match the designators for SHIFT, TIME, LAH, %, NULL and External Reference.
(54)	CALIBRATION SWITCH	Spring loaded pushbutton switch, accessible through hole in front panel. Switch is held depressed during software calibration to enter calibration constants into Non-Volatile Memory.
(55)	SIGN INDICATOR	LED illuminates to display the negative sign when the display reading is negative.
(56)	READ-RATE INDICATOR	Front panel LED indicator that illuminates when the DMM takes a reading.
(57)	POWER SWITCH	Push-on, Push-off type switch on front panel.

Table 3.2 - Rear Panel Terminals and Control

Reference	Designator/Label	Functions
(1)	Ω SOURCE BANANA JACK	Ω Current Return (J206).
(2)	INPUT HI BANANA JACK	+ Signal Input (J207).
(3)	SYNC OUTPUT BNC CONNECTOR	Outputs negative going TTL pulses each time a reading is displayed. Used to synchronize input scanners, such as Racal-Dana 1200.
(4)	FUSE HOLDER	.5 Amp "Slo-Blo" (115V). .25 Amp "Slo-Blo" (220V).
(5)	AC POWER PLUG	Accepts Racal-Dana AC cord 600620., and European standard cord P/N 600858.
(6)	ADDRESS SWITCH	GPIB ADDRESS SWITCH. DMM bus number selector.
(7)	GPIB CONNECTOR	GPIB port (J201).
(8)	EXTERNAL TRIGGER BNC CONNECTOR	A negative going TTL level pulse applied to this connector initiates a measurement cycle when in " Hold " mode.
(9)	LINE VOLTAGE SELECTOR WINDOW	The selected AC voltage viewing window.
(10)	GUARD BANANA JACK	Rear panel connector to internal guard shield (J205) connected internally to front panel guard connector (J101).
(11)	INPUT-LO BANANA JACK	–Signal Input (J204).
(12)	Ω SOURCE BANANA JACK	Ω Current Source (J203).
(13)	EXT. REF HI-BANANA JACK	External Reference INPUT. HI-J211.
(14)	EXT. REF LO-BANANA JACK	External Reference INPUT LO-J201.

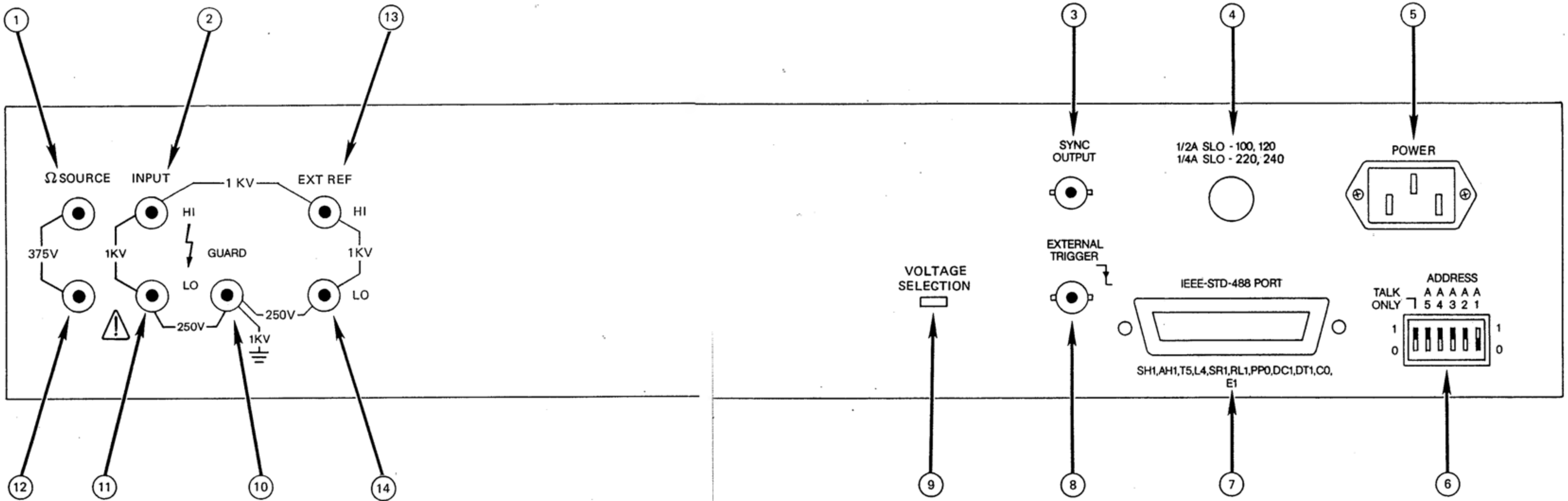


Figure 3.2 - Rear Panel

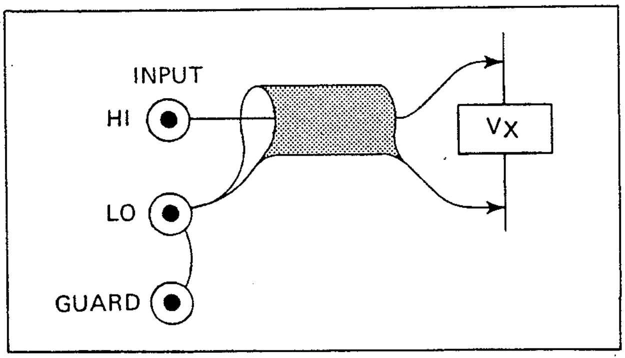


Figure 3.3 - DC, AC Measurement Connections Using Coaxial Cable

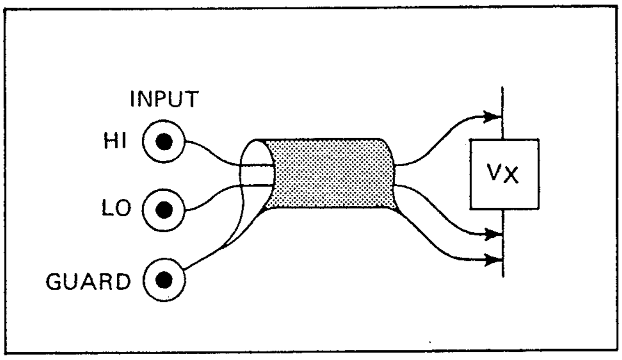


Figure 3.4 - DC, AC Measurement Connection Using Two Conductor Shielded Cable

3.4.3 DC Volts Measurements.

3.4.3.1 The basic instrument is capable of measuring DC volts in 5 ranges: 0.1V, 1V, 10V, 100V, 1000V. To measure DC voltage proceed as follows:

3.4.3.2 Complete the DMM turn-on procedure as described in paragraph 3.2.2, then check the zero accuracy of the instrument as described in paragraph 3.4.1.

3.4.3.3 Connect the DC voltage to the INPUT HI-LO terminals, refer to Figure 3.3 and Figure 3.4, and read the value from the display and range annunciators.

3.4.4 AC Volts Measurements.

3.4.4.1 The DMM is capable of measuring AC volts in 4 ranges: 1V, 10V, 100V, 1000V. To measure AC voltage proceed as follows:

3.4.4.2 Complete the DMM turn-on procedure as described in paragraph 3.2.2.

3.4.4.3 Select the AC volts function by pressing the AC key, then verify that the AC annunciator LED is on.

3.4.4.4 Connect the AC voltage to the INPUT HI-LO terminals, refer to Figure 3.3 and Figure 3.4, and read the value from the display and range annunciators.

3.4.4.5 AC Voltage measurements for the Model 5005 Averaging AC to DC Converter are always AC coupled (DC component of input is blocked). For the Model 5006 True RMS to DC Converter, AC Voltage Measurements can be made either as AC coupled or DC coupled.

3.4.4.6 To select DC coupled operating (AC + DC mode) for the 5006 AC converter, proceed as follows:

a) Set DMM power switch to off.

> **WARNING**
> These instructions are for use by qualified personnel only. To avoid electric shock, do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so.

b) Unplug power cord.
c) Remove top cover (see 2.5.1.2).

> **WARNING**
> Removal of covers exposes potentially lethal voltages. Avoid contact with internal electrical connections while unit is connected to AC power source.

d) Extract RMS Converter and remove top guard shield on converter board.
e) Set S1 and S2 switches to DC (toward center of board).
f) Replace guard shield and reinstall RMS Converter in unit.
g) Install top cover (see 2.5.1.5).
h) Set connect power cord and set AC power switch to ON. To select AC coupled operation, perform steps (a) through (h) above, but in step (e), set S1 and S2 switches to AC (away from center of board).

3.4.5 Resistance Measurements.

3.4.5.1 The DMM is capable of measuring resistance values in six ranges, starting at 100 ohms full scale to 10,000,000 ohms full scale. The correlation between the front panel keyboard and resistance selection is best described by the chart that compares range designators and resistance scales, as follows:

a) When the KΩ function is selected, the range keys carry a scaled factor of 1000 or range key "1" equals one thousand ohms full scale.
b) Range keys and resistance measurement comparison:

Range Key	Ohms - Full Scale	
.1	100	Ohms
1	1000	Ohms
10	10,000	Ohms
100	100,000	Ohms
1K	1,000,000	Ohms
10K	10,000,000	Ohms

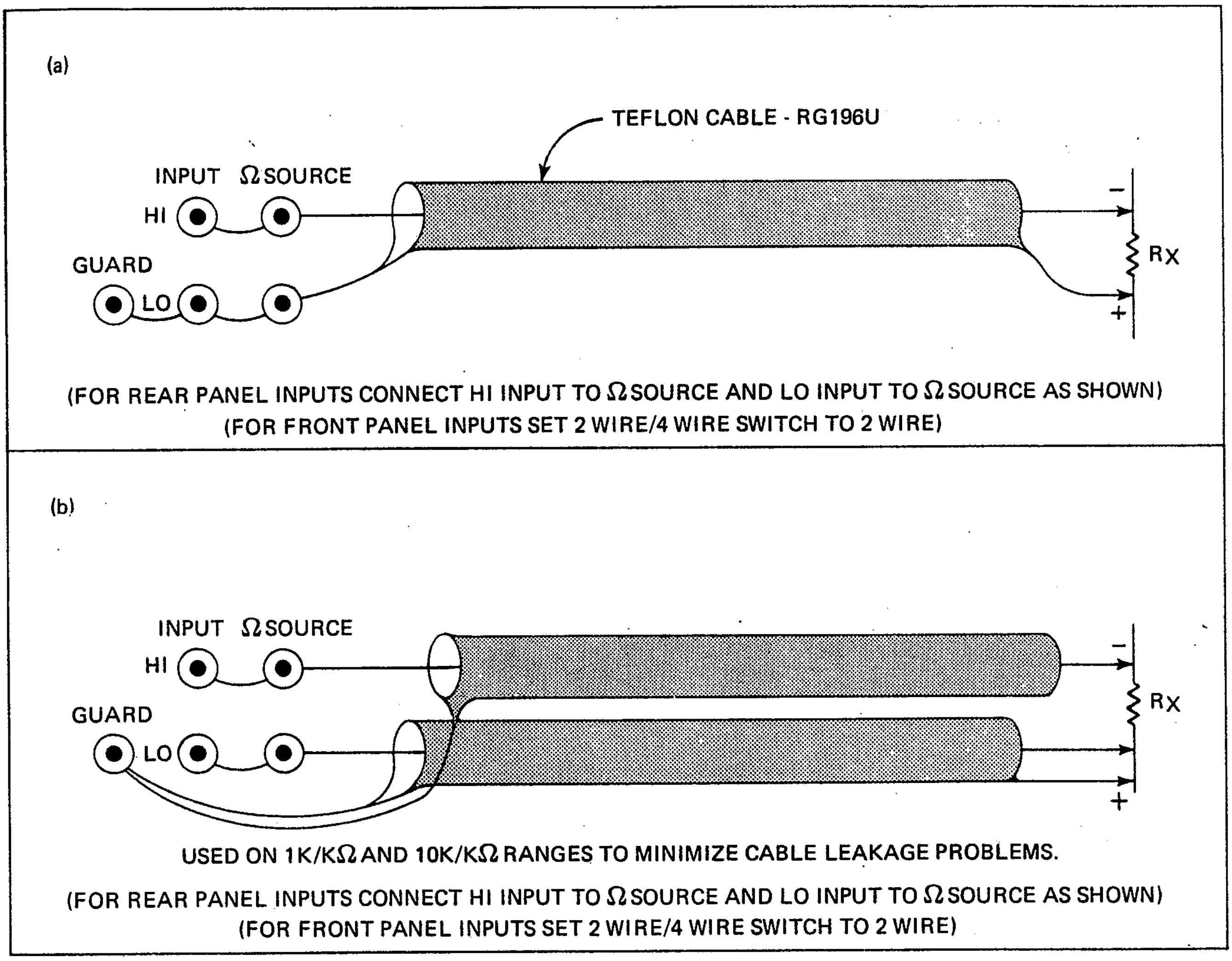


Figure 3.5 - Two Wire Ohms Measurements

3.4.5.2 Furthermore, the operator has the option of selecting two-wire or four-wire mode of operation through the front panel switch, No. 30 on Figure 3.1. This selection is determined by the accuracy required by the User and the environment. The application and description for each system is described in the procedures that follow.

3.4.5.3 Two-Wire measurements through the Front or Rear Panel INPUT terminals are connected as shown in Figure 3.5A and 3.5B using Teflon shielded cable as indicated. The Two-Wire/Four-Wire switch on the front panel, No. 30 on Figure 3.1, is placed in the two-wire position, this automatically connects the Ohms Source terminals to the Voltage Input (sense) terminals. When rear terminal input is used, a jumper is required between the Ohms Source terminal and the HI Input, then another jumper is required between the other Ohms Source terminal and the LO Input terminal. These connections and the GUARD connection to LO input are shown on Figure 3.5. When performing polarity sensitive resistance measurements (e.g.semiconductor junctions), note the polarity of the voltage across the Ω SOURCE terminals (upper terminal is negative with respect to lower terminal).

3.4.5.4 Accurate measurements can be obtained with the two-wire system presented, except in the .1 and 1 ranges. At low resistance levels, lead resistance between Rx and the DMM can become a significant error factor. In this instance a four wire system is recommended to minimize lead resistance errors.

3.4.5.5 When measuring resistances in the 1K/KΩ and 10K/KΩ ranges, cable leakage may cause measurement errors if the connections of Figure 3.5A are used. The amount of inaccuracy will depend on the cable insulation and environmental conditions (e.g., high relative humidity, etc). For this reason, teflon insulation is recommended to minimize cable leakage. If teflon cable is not used, then the two wire cable wiring diagram of Figure 3.5B is recommended.

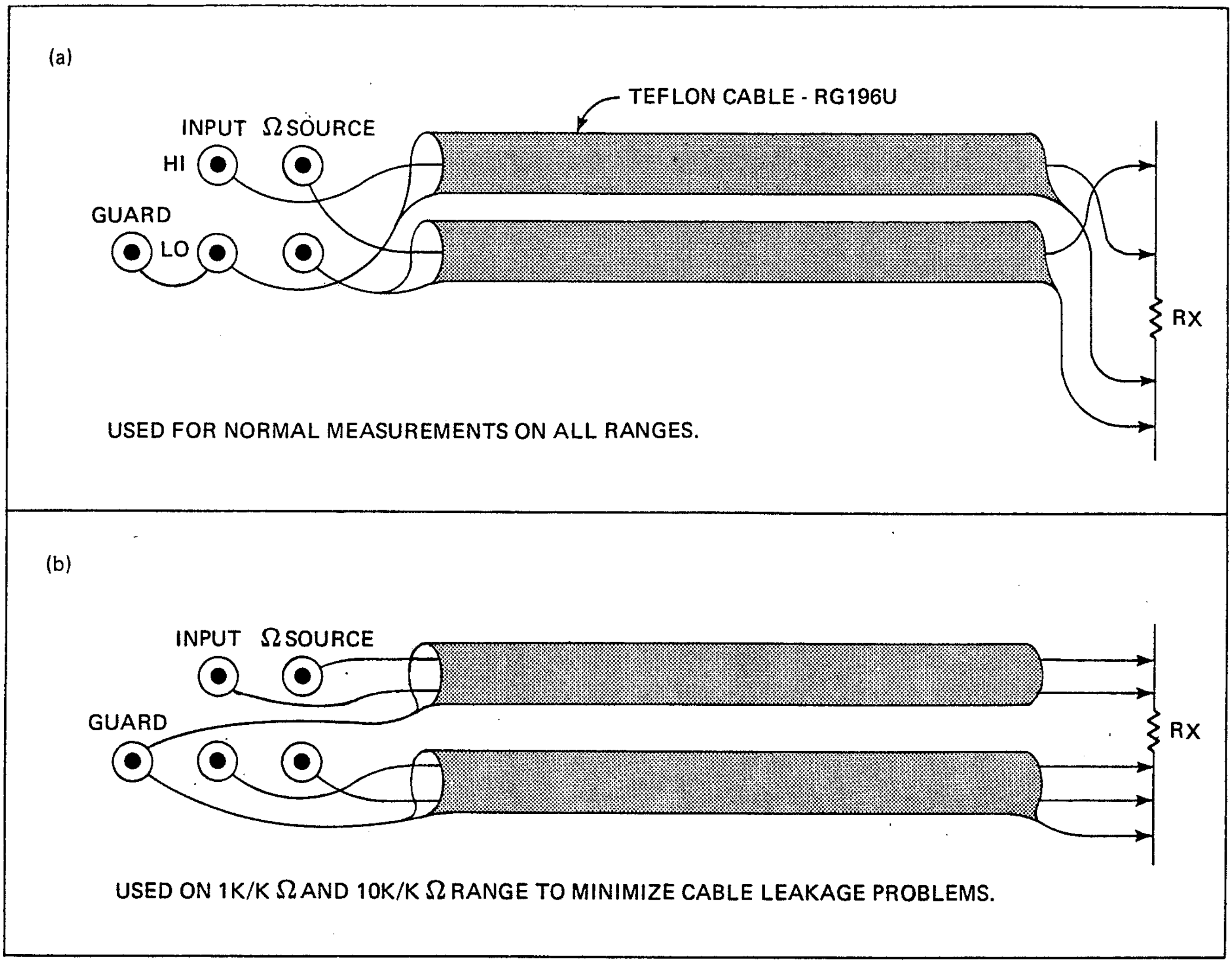


Figure 3.6 - Four Wire Ohms Measurement

3.4.5.6 Four Wire Measurement System is used in most systems applications, particularly where the device to be measured is at a remote location requiring interconnection by cables from several feet to hundreds of feet in length. When measuring low resistance values over long cables, most resistance problems can be resolved by the use of the four-wire measurement system.

3.4.5.7 The 2-Wire/4-Wire switch is set to 4-wire when front panel terminals are used for Four-Wire measurements. The four-wire resistance measurement diagrams are shown in Figure 3.6A and 3.6B. If teflon insulated coaxial cable is used, accurate measurements can be made on all ranges and under severe environmental conditions. Figure 3.6B shows the recommended connections when using two-conductor shielded cable. This wiring system eliminates most cable leakage problems when high resistances are measured with relatively high leakage cables.

3.4.6 DMM Extended Software Capability (ESC) Features.

3.4.6.1 The Extended Software Capability increases the program capabilities of the DMM. The features include NULL, %, LAH, TIME, Program Buffer and Data Buffer. The application and control description were presented in Section 3.3. Additional information continues in this section.

3.4.6.2 These programs were designed to operate either separately or in various combinations. For instance, the % and LAH function can be used together to determine average and worst-case percentage variations. In an another example, the Time Function and Data Buffer can be used together to monitor an input signal at pre-determined intervals and store the resulting readings for later recall. In general when two or more ESC features are enabled simultaneously, they will take place in the order shown in the ESC Feature Flow Chart, Figure 3.7.

3.4.6.3 When reviewing the Flow Chart, notice that the Time Function does not appear as a discrete block in this figure. The time function, if enabled, determines when a reading is permitted to take place; the reason will be seen later. A block for the Program Buffer was intentionally omitted since the program buffer affects the entire DMM's configuration, rather than each individual reading.

3.4.6.4 Keyboard operation which makes use of the STORE, RECALL, REF, or numeric entry keys causes the DMM to abort the sequence shown in Figure 3.7, and instead responds only to the keyboard input. When the operator has finished with keyboard operations, he can return to the Flow Chart sequence by pressing the SHIFT then CE (clear entry) keys. Other keys such as Function, Range or the RESET key may be used, but possible interaction may occur with the DMM's setup in various ways (see the description for each key in Table 3.1).

3.4.7 STORE and RECALL Procedures.

3.4.7.1 The STORE key is used in conjunction with other keys to store readings, numerical constants and Instrument Program Settings in the DMM's memory.

3.4.7.2 The general procedure for STORING READINGS is presented next:

a) If a reading is not presently displayed, depress the SINGLE or TRACK key.

b) Press the STORE key.

c) Press the key or keys which specify the storage location. The STORE key operations of the Extended Software Capability (ESC) features are listed in Table 3.3.

> **NOTE**
>
> If any ESC features are enabled, (NULL, %, etc.) the number stored will not match the number displayed. The ESC Flow Diagram presented in Figure 3.7 can be used as an aid to understand this phenomenon because the Flow Chart indicates that the Input Buffer contains the unprocessed reading rather than the output of NULL, Percent, etc.

3.4.7.3 STORING NUMERICAL CONSTANTS is presented next:

a) Press the SHIFT key, the SHIFT annunciator LED will illuminate.

b) Press the Numerical Entry Keys as required to enter the constant. The enteries will appear on the display.

c) Press the STORE key.

d) Press one of the key sequences shown in Table 3.3, Store Key Operations.

> **NOTE**
>
> If an error is made keying the STORE procedure, press SHIFT and clear entry (CE) keys to return the DMM to its previous state.

3.4.7.4 The RECALL KEY is used in conjunction with other keys to examine data which is stored in the DMM's memory and to recall Instrument settings from the program buffer. The RECALL Key sequences in Table 3.4 show all the possible sequences, along with other details.

> **NOTE**
>
> If any error is made keying the RECALL procedure, press the SHIFT and clear entry (CE) keys to return the DMM to its previous state.

3.4.8 Low-Average-High Function.

3.4.8.1. The DMM provides a Low-Average-High (LAH) measurement capability. When used in this mode the instrument performs the following operations:

a) Stores the least positive (or most negative) value measured during LAH operation;

b) Stores the value of the most positive (or least negative) measurement made during LAH operation;

c) Calculates the average value of all measurements taken during the LAH average cycle;

d) Counts the number of measurements taken during the LAH average cycle.

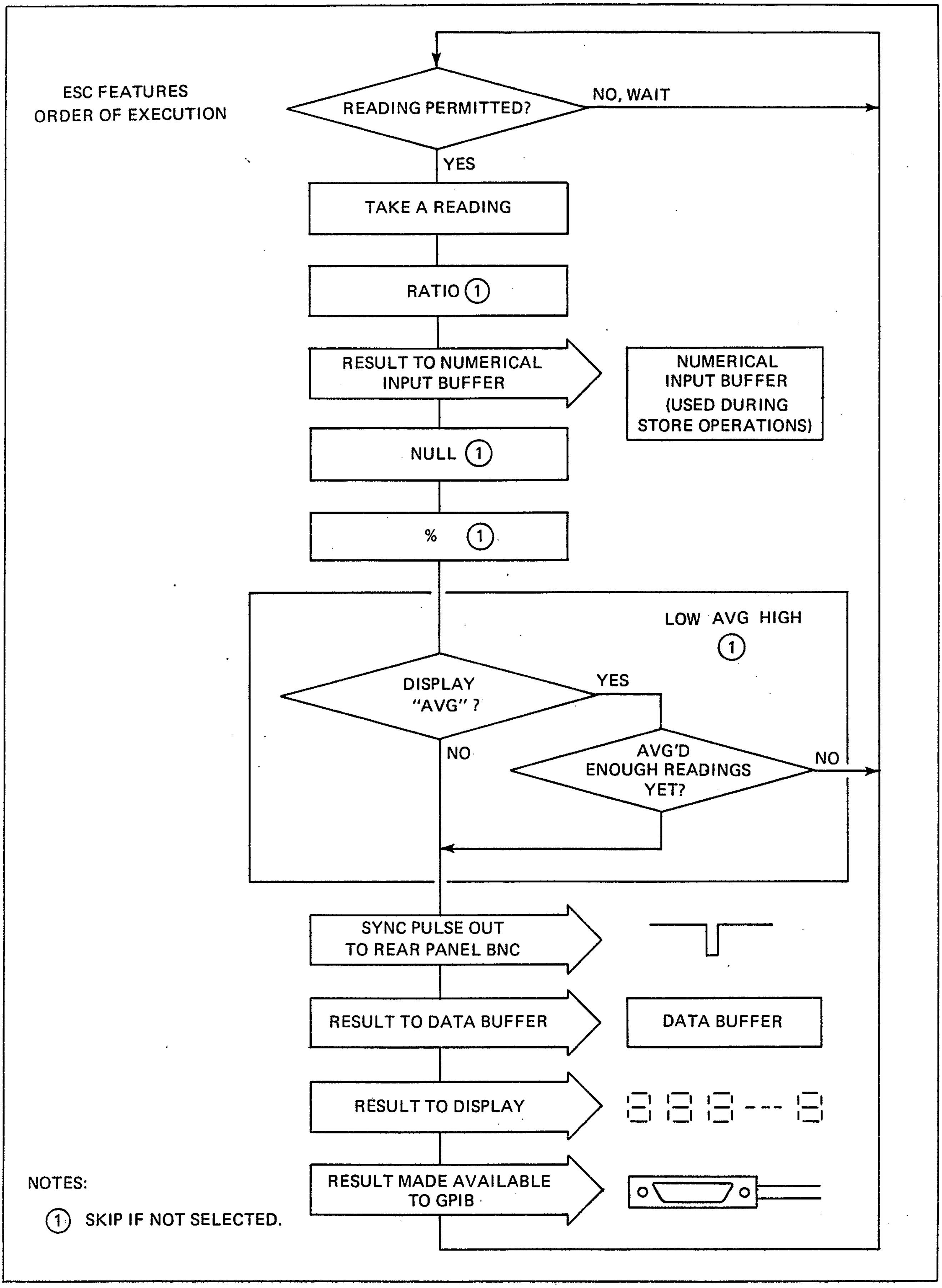


Figure 3.7 - Extended Software Capability Feature Flow Chart

Table 3.3 - Store Key Operations

Key Sequence	Storage Location	Power-Up Value	Units	Notes	For More Info See Paragraph
STORE □ NULL □	Null Constant	0.00	Volts or Kohms	Null Function should be enabled before Null constant is stored.	3.4.10
STORE □ % □	Percent Constant	0.00	Volts or Kohms		3.4.11
STORE □ LAH □	LAH Average Cycle Count C	4	Dimensionless	C, the LAH Average cycle constant should be between 1 and 10,000. If C = 10,000 A and N will not periodically reset.	3.4.8
STORE □ TIME □ 1 □	Start Time	00.0000	Hr. Min Sec	(1)	3.4.9
STORE □ TIME □ 2 □	Stop Time	99.0000	Hr. Min Sec	(1)	
STORE □ TIME □ 3 □	Interval	00.0000	Hr. Min Sec	(2)	
STORE □ TIME □ 4 □	Subinterval	00.0000	Hr. Min Sec	(2)	
STORE □ TIME □ 5 □	N (number)	1	Dimensionless	(3)	
STORE □ TIME □ 6 □	Present Time	00.0000	Hr. Min Sec	(1) (4)	
STORE □ SHIFT □ 9 □ . . . 0 □	Program Buffer	Empty	N/A	Stores the entire DMM's present setting into the Program Buffer, and initializes the Data Buffer.	3.4.12

Notes for rows with paragraph 3.4.9:

(1) A time-of-day number which should be set between 00.0000 and 95,5959 for normal operation, or set greater than 95.5959 to place constant at infinity on time scale.

(2) An elapsed-time constant same numerical limits apply as in (1)

(3) An Integer, normally set between 1 and 99

(4) Automatically increments to track the passing of time.

Table 3.4 - Recall Key Operations

Key Sequence	Recall Location	Power-Up Value	Units	Notes	For More Info See Paragraph
☐ RECALL ☐ NULL	Null Constant	0.00	Volts or Kohms		3.4.10
☐ RECALL ☐ %	Percent Constant	0.00	Volts or Kohms		3.4.11
☐ RECALL ☐ LAH L	Lowest Reading	Blank Display	Volts or Kohms	(1) — (1) A blank display indicates that no answer is presently available (answer is "the empty set"). (2) Automatically initialized every C readings.	3.4.8
☐ RECALL ☐ LAH A	Average Reading	Blank Display	Volts or Kohms	(1)(2)	
☐ RECALL ☐ LAH H	Highest Reading	Blank Display	Volts or Kohms	(1)	
☐ RECALL ☐ LAH n	Number of Readings	0	Dimensionless	(2)	
☐ RECALL ☐ LAH C	Average Cycle Constant	4	Dimensionless		
☐ RECALL ☐ TIME 1 ☐	Start Time	00.0000	Hr. Min Sec		3.4.9
☐ RECALL ☐ TIME 2 ☐	Stop Time	99.0000	Hr. Min Sec		
☐ RECALL ☐ TIME 3 ☐	Interval	00.0000	Hr. Min Sec		
☐ RECALL ☐ TIME 4 ☐	Subinterval	00.0000	Hr. Min Sec		
☐ RECALL ☐ TIME 5 ☐	N (number)	1	Dimensionless		
☐ RECALL ☐ TIME 6 ☐	Present Time	00.0000	Hr. Min Sec		
☐ RECALL ☐ BUFF			Volts or Kohms	Number at right side of display during pressing of BUF key indicates buffer location #.	3.4.12
☐ RECALL ☐ SHIFT 9 ☐ . . . 0 ☐			N/A	Programs entire instrument to setting previously stored in locations 0-9.	3.4.12

3.4.8.2 The length of the LAH average cycle is determined by an operator entered number using the procedure described in paragraph 3.4.8.4. The number entered will equal the number of readings the operator wants to average in each LAH average cycle up to a maximum of 10,000. If selected for display, a new average is displayed at the end of each LAH average cycle. However, the low and high values are derived from all readings taken since the LAH function was selected.

NOTE

The LAH function will update the minimum and maximum readings indefinitely, but will not update the average or the number of measurements readings beyond the first 10,000 samples.

3.4.8.3 The operator may select the lowest (most negative) measurement (L), average measurement (A), highest (most positive) measurement (H), number of measurements (n), or the present reading (r) to be displayed while the LAH function is selected. The desired display selection is described in the following procedure:

a) Depress and hold the LAH key. As long as the key is depressed, the display will repeat the sequence "L, A, H, n, r" in the least significant digit location.

b) To display the most negative reading, release the LAH key while the "L" is displayed.

c) To display the average reading, release the LAH key while the "A" is displayed.

d) To display the most positive reading, release the LAH key while the "H" is displayed.

e) To display the number of measurements taken during each LAH Average cycle, release the LAH key while the "n" is displayed.

f) To display the present measurement reading, release the LAH key while the "r" is displayed.

3.4.8.4 The desired number of measurements to be averaged during each LAH average cycle is programmed prior to entering the LAH function as follows:

a) Press the SHIFT key.

b) Key in the number of measurements to be averaged (e.g., press the 5 key and then the 8 key to select 58 measurements).

c) Press the STORE key.

d) Press the LAH key. The number of measurements constant (c) will remain in memory until it is changed or until power is removed from the instrument.

e) Select the desired display by following the procedure in the preceding paragraph. If the average reading is selected for display, the display will be updated each time the selected number of measurements is completed (e.g., every 58 measurements).

f) If the operator is not interested in using the LAH function's averaging capabilities, the LAH average cycle constant need not be initialized.

3.4.8.5 The operator, when using the RECALL key has access to the data stored during LAH operation. Press the key RECALL, then LAH and a letter will appear in the least significant digit location. Upon release of the LAH key, the letter will be replaced with the following corresponding data:

a) C: Number of readings averaged each LAH average cycle, operator entered as described in 3.4.8.4.

b) L: The least positive (most negative) reading that has occurred since the LAH function was selected.

c) A: The average computed over N readings (see N below).

d) H: The most positive (least negative) reading that has occurred since the LAH function was selected.

e) N: The number of readings taken during the present LAH average cycle.

NOTE

If the number of measurements to be averaged (C) is entered as zero, then the average will be taken over one reading (i.e., zero defaults to one), (C) will default to 10,000 if entered as >10,000. The number of measurements constant is initialized to four (C = 4) at power-up.

f) The Average is calculated and updated in memory as each reading is taken (up to 10,000). The average of "N" readings can be recalled before the average of " C " readings is displayed (if selected for display).

3.4.8.6 SYNC OUTPUT: As can be seen in Fig. 3.7, a pulse appears at the SYNC output each time the display is updated. When "average" is selected for display, the pulse will occur only once per LAH average cycle. Refer to paragraph 3.4.14.2 for a description of the SYNC output signal.

3.4.8.7 APPLICATIONS: A general list follows:

a) Low Frequency noise (less than 6 Hz) can be averaged resulting in a "quieter" display.

b) Lowest and Highest values can be captured during long term testing.

c) Using LAH and the % function allows the user to quickly determine the maximum, minimum and average % deviation for a quantity of electronic components.

3.4.9 NULL Function.

3.4.9.1 The NULL Function is an ESC feature of the DMM that can be enabled manually from the keyboard or through the GPIB remote system.

3.4.9.2 The NULL Function calculates and displays the difference between each measurement value and a Null constant. When NULL is enabled from the keyboard, *the number in the numerical input buffer, (see Fig. 3.7),* is stored as a NULL constant and subtracted from all future readings until changed or the NULL function is disabled by depressing the NULL key again. The NULL constant can be either the measurement value at the time NULL is enabled or a numerical value entered via the keyboard. A NULL constant can be entered from the keyboard when enabling Null operation or entered after the function is enabled. The operator can observe the Null constant in memory at any time by recalling it to the display.

3.4.9.3 To subtract the present reading from future measurements, simply depress the NULL key. The reading in the numerical input buffer, when the NULL key is depressed is stored as the Null constant.

3.4.9.4 To subtract a constant entered via the keyboard from each measurement value, execute the following keystrokes:

a) Depress the SHIFT key.

b) Key-in the numerics to be subtracted from each measurement value. This numeric will appear on the display as each key is depressed. If the Null constant is a resistance, enter the value in KΩ.

c) Depress the NULL key to store the numerical value as the Null Constant and simultaneously enable the Null Function.

3.4.9.5 To enter or modify the Null Constant after the Null Function is enabled, perform the following procedure:

a) If a measurement value is to be stored as the Null Constant, verify that a reading is presently in the display; if not, press the SINGLE or TRACK Key to take a measurement. Go to Step (c).

b) If a numerical constant is to be stored as the Null Constant, press the SHIFT Key and key-in the Null Constant with the numerical entry keys (these numerics will appear on the display). If the Null Constant is a resistance, enter the value in KΩ.

c) Depress the STORE key.

d) Depress the NULL key to enter the Null Constant into memory.

3.4.9.6 The NULL constant stored in memory can be recalled to the display anytime, with the two keystroke sequence RECALL and NULL.

3.4.9.7 The Null Function Applications are numerous but a few are listed as examples:

a) The measurement of line or load regulation of a DC power supply. The nominal DC output from the supply is substracted from its output under modified line or load conditions and the deviation displayed directly.

b) Cancellation of lead resistance in the measurement of low resistance values with a two-wire connection to the unknown resistance.

c) Addition or subtraction of a constant from the measured value. Addition is accomplished by entering the Null constant with a minus sign.

3.4.10 Percent Function.

3.4.10.1 The Percent Function complements the DMM's Extended Software Capability (ESC) features with the additions of percentage calculations when operating in the Volts and Ohms Functions. The Percent Function can be enabled manually from the keyboard or through the GPIB system.

3.4.10.2 The Percent Function calculates and displays the percentage deviation of each measurement and from a reference value (Percent Constant). The deviation calculation formula is:

PERCENT DEVIATION =

$$\frac{\text{Measurement Value - Percent Constant}}{\text{Percent Constant}} \times 100$$

The Percent Function is enabled or disabled, by pressing the Percent (%) key when not preceded by the STORE or RECALL key. However, a non-zero percent constant must be stored to obtain meaningful results. The "%" annunciator indicates when the function is enabled.

3.4.10.3 The Percent Constant can be either a measurement reading or a numerical value entered via the keyboard. Note that an "ERROR 0" message is displayed, when a Percent Constant is not stored in memory prior to enabling the Percent Function. The operator can check the Percent Constant in memory by recalling it to the display, following the instructions listed in Table 3.4 and paragraph 3.4.7.

3.4.10.4 To store a measurement value or numerical constant as the percent constant, perform the following procedure:

a) If a measurement value is to be stored as the Percent Constant, verify that a reading is presently in the display; if not, press the SINGLE or TRACK key to take a measurement. Go to step (c).

b) If a numerical constant is to be stored as the Percent Constant, press the SHIFT key and key-in the Percent constant with the numerical entry keys (these numerics will appear on the display).

c) Depress the STORE key.

d) Depress the % key to store the displayed number into memory. Note that pressing the % key did not enable or disable the Percent Function because it was preceded by the STORE key. If this procedure is performed while the Percent Function is enabled, the calculation and display of Percent Deviation will begin with the next reading.

3.4.10.5 Percentage Deviations too large to display normally will be displayed in Scientific Notation, (e.g., 1,000,000% displayed as 1.00E6). However, percent deviations equal to or greater than 10^{10}% will result in an "ERROR 6" message. Other conditions related to the number of significant digits in the calculated value will also cause the percentage to be displayed in scientific notation.

3.4.11 Time Function.

3.4.11.1 The Time function adds another dimension to the capabilities of the DMM by bringing measurement and computation features under the control of the DMM's built-in digital clock. It also gives the user a very useful 96 hour clock which can be used when the DMM is not otherwise employed. The Time function can be configured to provide timed measurements with selectable Start time, Stop time, Interval, Subinterval, Number of Readings (N), and Present Time. Most applications will require only a subset of the Time function's full capabilities.

3.4.11.2 The Time function when used in conjunction with other Extended Software Capability Features, increases the DMM's applications. The following list describes typical applications:

a) Monitor an input signal at programmed intervals up to 96 hours and beyond.

b) Store all readings into the Data Buffer for later recall.

c) The sync output can sequence a scanner (such as Racal-Dana's Model 1200) to scan up to 99 inputs at controlled intervals and store the readings to the Data Buffer as well as output them to a GPIB printer.

d) When used in conjunction with LAH function, it can be used to average up to 10,000 readings taken at controlled intervals.

3.4.11.3 The TIME function key on the keyboard is a toggle switch which is depressed to toggle "ON" and depressed again to toggle "OFF". When the Time key is toggled ON, it puts the DMM into hold. When the Time key is toggled OFF, it puts the DMM in the continuous reading mode. The Time annunciator will indicate the status of the Time key. When programmed from the GPIB, the trigger status is not affected by enabling or disabling the Time function. Further GPIB programming details are presented in paragraph 3.5.23.

3.4.11.4 There are six memory locations that control the various ways the TIME function operates. These memory locations, referred to in Table 3.5, have the indicated designators and limitations.

Table 3.5 - Time Register Codes

Name	Designator	Power-Up Initialization	Largest Value That The User Can Store	Comments
Start Time	Time 1	00.0000	99.5959	
Stop Time	Time 2	99.0000	99.5959	
Interval	Time 3	00.0000	99.5959	0 defaults to 1 second.
Subinterval	Time 4	00.0000	99.5959	
N (Number of Readings per interval)	Time 5	1	99	
Present Time	Time 6	00.0000	99.5959	Begins counting at power-up. Increments to 00.0000 at 96 hrs.

Note: The format for Time numbers is XX.YYZZ where XX = hours, YY = minutes, ZZ = seconds.

3.4.11.5 The Present Time Register is the most important of the six Time Function registers. At power-up the present time begins incrementing at one-second intervals until it reaches 95.5959 (95 hours, 59 minutes, 59 seconds.). One second later it resets to 00.0000 and begins incrementing again. Figure 3.8 shows the path taken by the Present Timer register as it approaches 96 hours on the time axis and then resets to zero. Note that the Present Time register always increments whether or not the Time function is enabled.

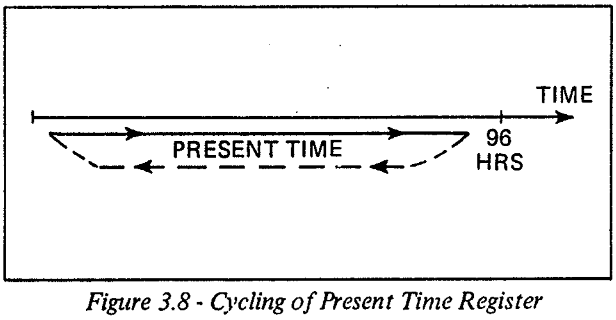


Figure 3.8 - Cycling of Present Time Register

3.4.11.6 The Start Time and Stop Time registers form a "window" during which readings can take place. As an example, Figure 3.9 shows the Start Time set to 20.0000 hours and the Stop Time set to 50.0000 hours. The example also shows how the Present Time has incremented past the Start Time, causing a reading to take place. Other readings may be triggered between start and stop times under control of the Interval, Subinterval, and N registers, which will be covered later.

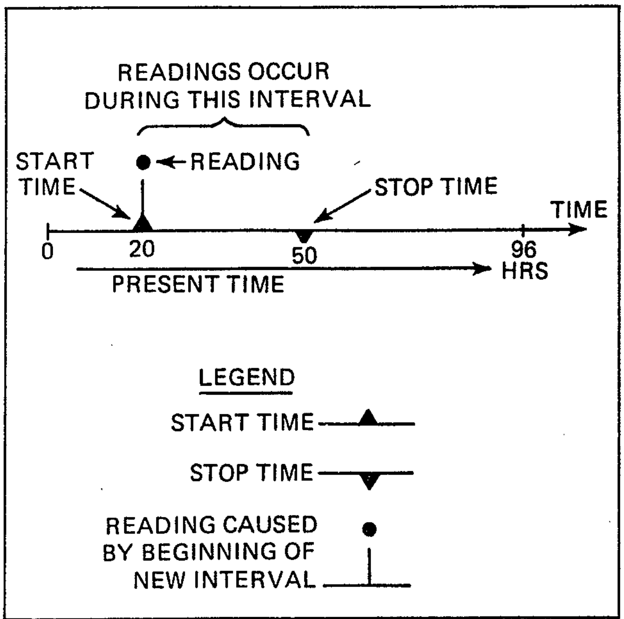


Figure 3.9 - Use of Start and Stop Time Register

3.4.11.7 Since the Present Time resets to zero at 96 hours, it is possible to set the Stop Time (or any other time register) at "infinity" on the time scale by storing a number greater than 95.5959 to the register in question. An example is shown in Figure 3.10, where the start time has been set to 30 hours and the stop time has been set to 99 hours, placing it "out of range" of the present time register. With these start/stop settings, reading(s) would begin at 30 hours and continue forever under control of the Interval, Subinterval and N registers.

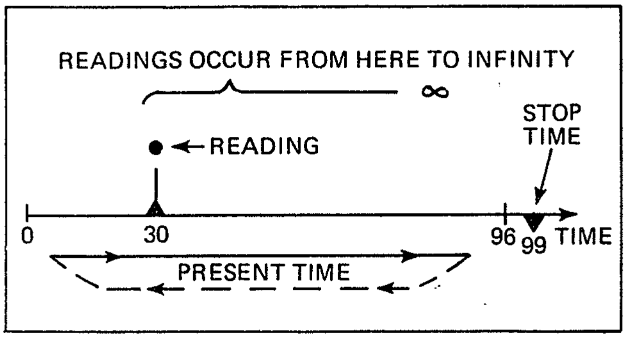
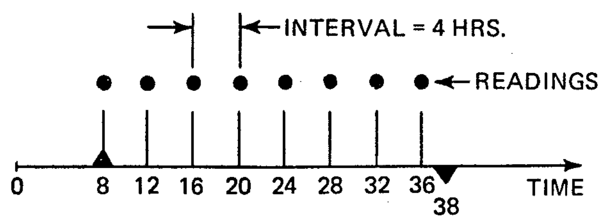


Figure 3.10 - Setting Stop Time at Infinity

3.4.11.8 Interval, Subinterval and N Registers: Once inside the Start-Time/Stop-Time window, the Interval, Subinterval and N registers control the triggering of readings. An example is shown in Figure 3.11, where the subinterval and N registers have been set to their power-up value and the Interval register is controlling the time between readings. Notice that once the Start Time is reached, the DMM's Interval register triggers a reading every Interval time until the Stop Time is reached.



REGISTER CONTENTS

START TIME	8.0000
STOP TIME	38.0000
INTERVAL	4.0000
SUBINTERVAL	0
N	1

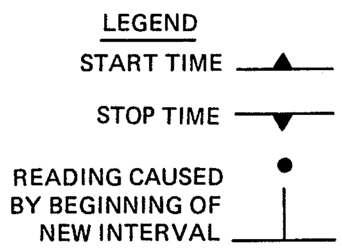
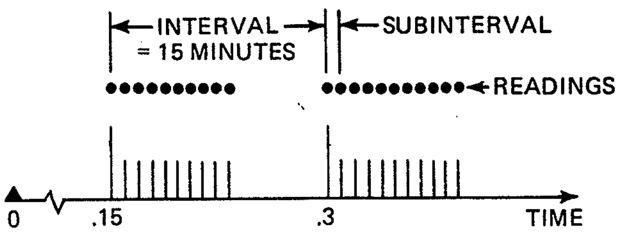


Figure 3.11 - Example of Start, Stop, and Interval Registers

3.4.11.9 Some applications require a read timing pattern similar to that shown in Figure 3.12. This read timing pattern is commonly used whenever a group of signals must be monitored within seconds of one-another periodically, as is the case when simultaneous temperature measurements must be made throughout a unit-under-test. Notice in this example that the Subinterval and N Registers are used to cause tight groups of 10 readings to occur every Interval time.



REGISTER CONTENTS

START TIME	0
STOP TIME	∞
INTERVAL	0.15 (15 MINUTES)
SUBINTERVAL	.0002 (2 SECONDS)
N	10 (10 RDGS/ INTERVAL)

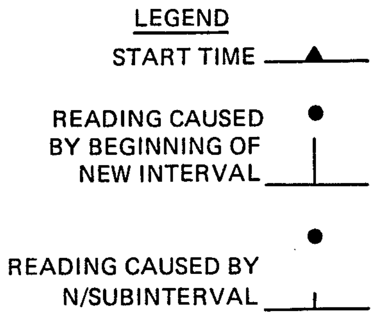


Figure 3.12 - Example of Interval, Subinterval and "N" Registers

3.4.11.10 Before the Time function is enabled, all 6 Time registers should be set to their proper values. Section 3.4.7 details the procedure for entering and storing all 6 Time constants. Keep in mind that hours are entered before the decimal point, minutes and seconds after the decimal point. Any Time constant can be examined by using the key procedure listed in Table 3.3. Recalling the Present Time allows the DMM's front panel display to be used as a 96 hour clock.

3.4.11.11 Some further points should be kept in mind when using the Time function:

a) If the Time function is disabled when the Present Time crosses the Start Time, readings will take place starting (1) Interval Time beyond the point when the Time function is enabled and continuing at Interval times from thereon. This is shown in Figure 3.13 where 2 identical Time function setups yield different results because of differences when the Time function is enabled. In order to avoid problems in critical applications, make sure that the Time function is enabled before the Present time encounters the Start time.

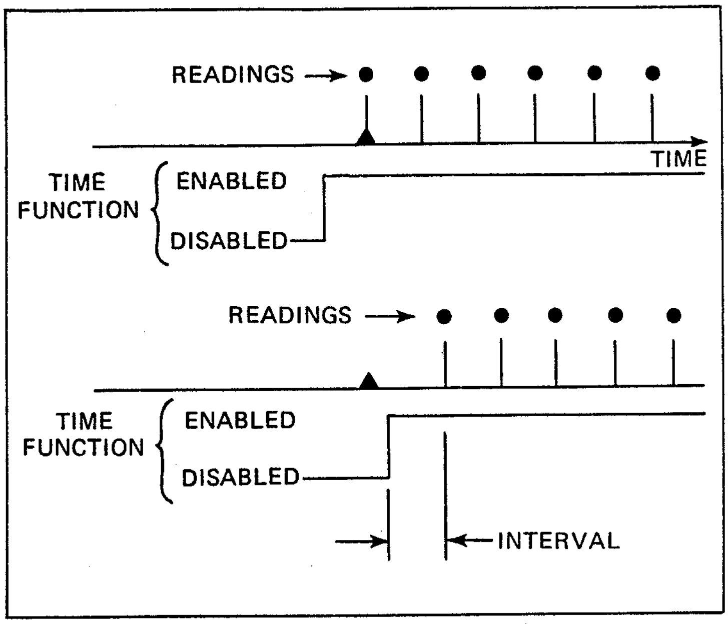
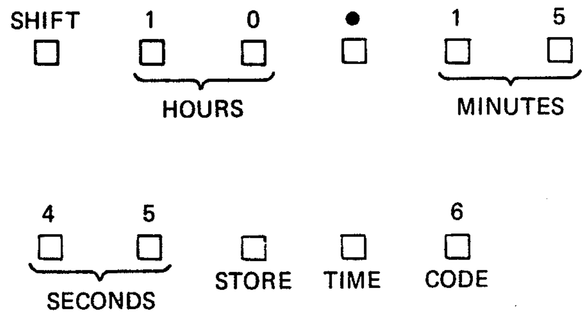


Figure 3.13 - Effect of Enabling Time Function After Start Time

b) The accuracy of the Time function is ± [(2 seconds/ hour) + 1 second].

c) Many front panel keyboard operations can disrupt the Time function. Therefore, the DMM should be completely set up before enabling the Time function.

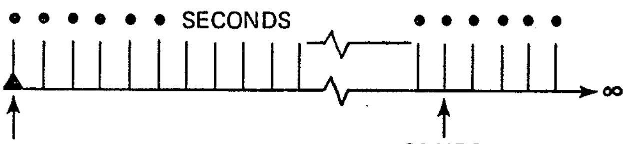
3.4.11.12 The following example lists the key strokes required to alter the Present Time (TIME6) to 10 hours, 15 minutes, and 45 seconds:



The SHIFT key enables the numeric key settings of 10 hours, 15 minutes and 45 seconds, this is followed by the STORE key, TIME key, and the last numeric entered sets the "N" register to be altered.

3.4.11.13 The following text represents a group of TIME Function examples and applications:

a) Pressing the TIME key without storing times in Time Registers will result in processing one reading per second (Time Registers are in their Power-up state). Note that TIME 3 (Interval) defaults to 1.0 second when no other value is stored.

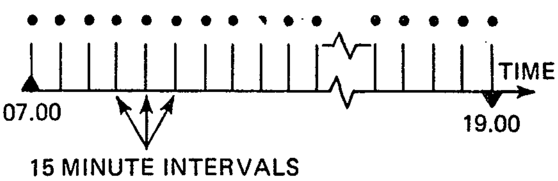


PRESENT TIME	00.0000
START TIME	00.0000
STOP TIME	99.0000
INTERVAL	00.0000
SUBINTERVAL	00.0000
N	1

b) For most applications the N and Subinterval will be left at their power-up values. As an example, suppose we wish to measure the AC line voltage every 15 minutes from 7:00 AM to 7:00 PM. The registers would be loaded as follows:

Start Time	(Time 1)	07.0000
Stop Time	(Time 2)	19.0000
Interval	(Time 3)	00.1500
Present Time	(Time 6)	Some real-time before 07.000.

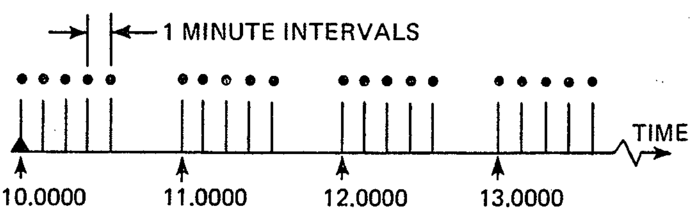
Graphic example:



c) To process 5 readings taken one minute apart, every hour, on the hour, starting at 10:000; the registers are set up as follows:

Present Time	(Time 6)	Some real-time before 10:00.
Start Time	(Time 1)	10.0000
Stop Time	(Time 2)	99.0000
Interval	(Time 3)	01.0000
N	(Time 5)	05.0
Subinterval	(Time 4)	00.0100

Graphic example:



3.4.12 External Reference (Software Ratio) Measurements

3.4.12.1 The External Reference, software ratio measurements are an ESC feature of the DMM that configures the DMM to function as a ratiometer. Ratio measurements are made by applying a DC or AC external reference voltage to the DMM's EXT REF input terminals located on the rear panel, and selecting the appropriate external reference function and external reference range. Section 3.5.29 and Table 3.12 give descriptions of the GPIB program codes required to enable the software ratios. Upon selecting the Software Ratio mode, the DMM reads the measurement signal, the external reference signal, then calculates:

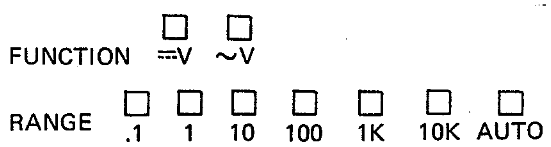
$$\text{RATIO} = \frac{\text{Measurement Signal}}{\text{External Reference Signal}}$$

3.4.12.2 The selection of the Reference Function/Range is completely independent of the Measurement Function/Range, therefore, over 100 types of Software Ratios can be programmed. A few examples are:

$$\frac{\text{AC-10V Range}}{\text{DC-1000V Range}}, \quad \frac{\text{AC 1V Range}}{\text{AC 1V Range}} \text{ and } \frac{\text{Ohms .1 Range}}{\text{DC-100V Range}}$$

3.4.12.3 To select the External Reference Function/Range, the REF key is depressed to enable or disable the external reference mode. When enabled, "REF" is displayed on the DMM's front panel and the annunciator LED's display the present reference function and range in the REF mode, if all the function LED's remain blank, then this indicates that the DMM's internal reference was selected, that is, the DMM is in its "normal" measurement mode.

3.4.12.4 While in the REF mode, an external reference function or range can be selected. This is done by pressing a function or range key. The following keys will modify the reference function or range setting:



The annunciatorLED's will then indicate the new reference setting.

3.4.12.5 Once the reference function and range are selected, the REF key is pressed to exit the REF mode, also the DMM begins taking readings. The EXT REF LED will be ON if an external reference function was selected. When the LED is OFF, then the DMM is using its internal reference

3.4.12. The user can return to Internal Reference by pressing a Function key when not in the REF mode or by pressing the RESET key at any time. To examine the Reference settings without distributing it, press the REF key to enter the REF mode, examine the Function and Range annunciators, and then press the REF key again to exit the REF mode.

3.4.13 Program and Data Buffers.

3.4.13.1 The DMM 5004 contains a large area of Random Access Memory (RAMS U22 and U31) which is dedicated to the storage of instrument settings and readings. The instrument settings which refer to the position of all controls are stored in the Program Buffer and the readings which the DMM generates are stored in the Data Buffer.

3.4.13.2 THE PROGRAM BUFFER.

3.4.14.2.1 The Program Buffer allows the user to:

a) STORE ten complete instrument settings either as keyboard inputs or as GPIB inputs. The stored instrument settings can include Function, Range, Trigger, NULL, LAH, Percent, Time and numeric constants associated with the above mentioned ESC features.

b) In any sequence, RECALL the settings which were previously stored into the Program Buffer.

3.4.13.2.2 The ten Program Buffer registers will power-up in an 'empty' or initialized state, therefore instrument settings must be stored into the buffer before attempting to recall "program settings" from the buffer. To store a setting into the program buffer from the keyboard, (GPIB procedure is described in paragraph 3.5.9) the following procedure is used:

a) Keyboard Input: Program the DMM to the setting that will be stored in the buffer. For example, if Buffer program No. 9 will be DC, Auto-range and LAH function, depress the DC, AUTO and LAH keys, and continue with (b) next.

b) Press ☐ STORE Key.

c) Press SHIFT ☐ Key.

d) Press 0 ☐ .. 9 ☐ key as required.

During step d, the 7-segment display will display the message "ProGX" where X is the selected storage location (0-9).

3.4.13.2.3 There are some points to consider when "storing" programs to the Program Buffer:

a) Whenever a program is stored to the program buffer, the Data Buffer is cleared.

b) Programs can be redefined at any time. For example, the Program No. 9 contents can be changed to some other setting by first selecting the appropriate functions (using keyboard or GPIB) and then storing to program No. 9 again.

c) Once a program location is stored, it remains defined until the power is switched OFF to the DMM.

d) If the operator plans to use the Data Buffer, he should avoid storing programs to more program locations than necessary, otherwise the Data Buffer will become restricted in size. For further details, refer to paragraph 3.4.12.4, the Buffer Organization.

3.4.13.2.4 The following procedure is used to RECALL a program stored in the Program Buffer:

a) Press ☐ RECALL key.

b) Press SHIFT ☐ key.

c) Press 0 ☐ .. 9 ☐ key as required.

During step "C" the 7-segment display will show the message "ProGX" where X is the selected program location (0-9). When the RECALL procedure is completed, the DMM will immediately assume the settings which have been recalled from the program buffer.

3.4.13.2.5 Consider the following points when "recalling" programs from the Program Buffer.

a) Whenever a program is recalled, the LAH function is cleared. This is done so that if the recalled program makes use of LAH, the LAH constants which are generated will not be affected by the previous instrument settings.

b) All of the Time Function registers will be affected by a program recall with the exception of T6, the present time.

3.4.13.3 THE DATA BUFFER.

3.4.13.3.1 The Data Buffer allows the user to:

a) Store over 130 readings for later use.

b) Recall these readings to the display or over the GPIB.

c) The Data Buffer can store over 130 readings when the Program Buffer is not in use and over 45 readings can be stored when all 10 Program Buffers are used. This is described in Section 3.4.12.4 which discusses Buffer Organization.

d) The Data Buffer is a first-in-first-out (FIFO) register; therefore during recall location Ø contains the first stored reading, location 1 contains the second, etc.

3.4 .3.2 Unlike most ESC features of the DMM, the Data Buffer cannot be disabled or "turned-off"; therefore it is always either in the storing process or the register capacity is completely filled. The two operations which can be performed on the buffer are clearing (CE) and recalling (RECALL). Everytime that a reading is taken, it is first processed by other ESC functions such as NULL, %, and LAH. Then the Data Buffer is checked for space availability. If available, a copy of the processed reading is stored into the buffer. The buffer will remain filled until cleared and the readings from the buffer can be recalled any number of times to the display or the GPIB.

3.4.13.3.3 The Data Buffer will power-up in the cleared or empty state. Therefore data readings must be taken or accumulated in the buffer before attempting to recall the data readings from the Data buffer otherwise the DMM will either show mostly a blank display to a bench operator or send an SRQ to the controller if in remote. In order to prevent the Data Buffer from being accidentally cleared from the keyboard (GPIB procedure is described in paragraph 3.5.28) a time delay is inserted in the Keyboard Buffer Clear routine. To clear the Data Buffer, the BUFF key must be depressed until the seven-segment display shows the entire word "ClrbuF". This should take about five seconds.

3.4.13.3.4 The recalling of readings from the Data Buffer to the display (GPIB procedure is described in paragraph 3.5.9) can be accessed sequentially and displayed on the DMM's front panel by following the procedure listed below:

a) Press the RECALL key. The display will show "rCL".

b) Press the BUFF key. A number will appear at the right edge of the display, assuming that the buffer is not completely emptied or cleared. This number is the buffer address that will be recalled when the BUFF key is released. Depressing the BUFF key for two seconds enables the displayed address to increment and will eventually reach the point where the last reading was stored. The displayed address will then return to zero and begin incrementing up again. If the user wishes to initialize the recall process to address the first constant, the procedure listed next should be followed.

1) DO NOT DEPRESS THE RECALL KEY.

2) Depress the BUFF key and monitor the display.

3) The display will show "Clr" as the BUFF key is depressed. Release the key after appearance of the r in "Clr".

4) This will initialize the recall address to 00.

3.4.13.4 BUFFER ORGANIZATION.

3.4.13.4.1 By allowing the two buffers to share the same memory, more readings can be stored into the data buffer (over 130) when the program buffer is not in use. This is best described by reviewing Figure 3.14A and Figure 3.14B which show the relation between Program and Data buffers.

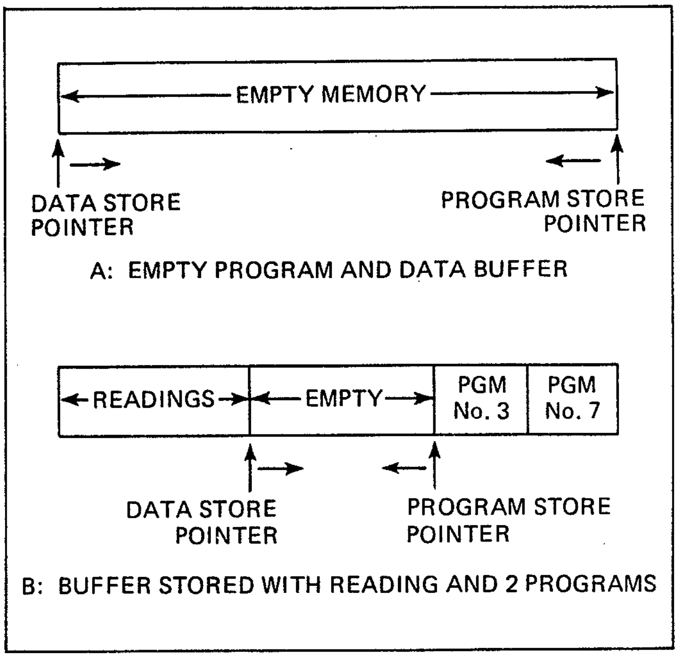


Figure 3.14 - Program and Data Buffer Storage

3.4.13.4.2 There are two pointers associated with the buffer operation as shown in Figure 3.14. The Program Store pointer points to the next available program storage location, moving right to left as programs are stored. The Data Store pointer points to the next available data storage, moving left to right as readings are stored. The Data Store pointer bumps into the Program Store pointer when the memory block is full. Hence, no more readings are stored until the data buffer is cleared.

3.4.14.4.3 When the Program and Data Buffers are used simultaneously, the Data Buffer must operate with a smaller memory space, as shown in Figure 3.14B. From the figure, it is noted that program No. 7 and program No. 3 have been stored in the buffer. This has reduced the number of readings which can be stored.

3.4.13.4.4 Data Buffer size can be determined when Data and Program Buffers are used simultaneously. The following equation can be used to determine the number of readings which can be stored:

No. of Readings = 130 – (7·N)

where N is the number of programs which were stored (N = 2 in Figure 3.14B).

3.4.14 Error Messages.

3.4.14.1 Error messages are classified in two categories, General Error Messages and GPIB Error Messages. The general error messages with numerics 0 through 9 apply to local and remote operations. GPIB error messages with numerics 10 through 13 apply only to remote operation.

3.4.14.2 For local operation, the DMM employs the 7-segment display to exhibit the error message code numbers. The error message numbers and explanations are listed in Table 3.6; General and Remote Error Messages.

3.4.14.3 For remote GPIB operation, the DMM transmits an SRQ to the controller; the controller replies with the "Y" program code to the DMM to request the error message number. The remote error message numbers and explanations are listed in Table 3.6. Refer to Section 3.5.20 for further explanation of the "Y" program code.

Table 3.6 - General and Remote Error Messages

Error Message No.	Error Message
	GENERAL ERROR MESSAGES
0	Percent Constant: 0 during Percent calculations.
1	Not in the DC function, 0.1 range when executing DIGITAL ZERO command.
2	Attempting to execute DIGITAL ZERO command with an input voltage applied or the input open-circuited. Connect a short across input terminals and repeat DIGITAL ZERO command.
3	The microprocessor's on-board RAM is defective (U35 on the motherboard).
4	The contents of the non-volatile memory have been disrupted, therefore the instrument's calibration should be verified.
5	A digitizer offset greater than 1000 digits was measured during execution of DIGITAL ZERO command.
6	Percent Deviation of $\geq 10^{10}$% while in the Percent Function.
7	The RAM is defective, U22 and/or U31 on the motherboard.
8	An attempt was made to store a overload reading to a register inside the DMM or an attempt was made to store > 99.5959 hours into a Time function register.
9	At attempt was made to recall a program setting from the program buffer before setting was stored to the program buffer.
	GPIB ERROR MESSAGES
10	Recall of a constant whose value is empty set, for example - sending an "L7" command to a DMM will cause this error if the LOW, AVERAGE, and HIGH constants are the empty set (no readings taken yet.)
11	Triggered too fast or too often.
12	Syntax error during GPIB programming.
13	Option not installed.

3.4.15 DMM Pulse Level/Timing Characteristics.

3.4.15.1 EXTERNAL TRIGGER.

3.4.15.1.1 The signal level and timing requirements for the external trigger are presented in Figure 3.16A. These timing requirements are not critical when in local control as the DMM interprets a tight group of external triggers as a single trigger command and the rise and fall time specifications stated in Figure 3.16A do not apply, due to this internal debouncing. This allows the use of mechanical foot switches and other "noisy" signal sources with good results. When in remote, all external triggers are treated individually and two or more closely spaced triggers will cause the DMM to issue an SRQ to the bus and make an error message available to the controller.

3.4.15.2 SYNC OUTPUT.

3.4.15.2.1 The DMM provides a synchronizing output pulse from a BNC connector on the rear panel. Refer to Figure 3.2. This pulse, timing shown in Figure 3.16B, indicates when the DMM has finished a reading or a sequence of readings. This output pulse can be used to sequence a signal scanner or other device as shown in Figure 3.16C.

3.4.15.2.2 When Autorange is selected, the sync output will not appear until the DMM has completed autoranging, and has taken the reading on the proper range.

3.5 SYSTEM OPERATION.

3.5.1 This subsection presents information on the operation of the DMM in a system.

3.5.2 General Purpose Interface Bus.

3.5.2.1 The IEEE-488-1978 (GPIB) Interface provides remote programming for all controls and the output of data from the DMM. Inputs and outputs are made via a 24 pin connector, (see Figure 3.15), located on the rear panel. The pin location, line identification, and operation of the GPIB are in compliance with IEEE-STD-488-1978. The GPIB provides interface capability with other instruments and with a controller also utilizing the "interface bus" structure. Connector pin assignments are shown in Figure 3.17. The IEEE-488-1978 subsets available are listed in Table 3.7.

3.5.2.2 By assigning a unique address to the DMM, it can be "called up" by the controller or another device on the bus without interfering with other units on the bus. Switches located on the rear panel of the DMM permit the programming of the instrument address. The coding used for the address is binary. Any one of 31 codes can be used for the address of an instrument, but a total of 15 is the maximum number of devices that can be used on one bus.

Table 3.7 - IEEE-488-1978 Standard Interface Subset Capability

GPIB Subset	Description	Applicable Capability
SH1	Source Handshake	Complete Capability
AH1	Acceptor Handshake	Complete Capability
T5	Talker	Complete Capability (1) Basic Talker (2) Serial Poll (3) Talk only Mode (4) Unaddress if MLA
TE0	Extended Talker	None
L4	Listener	Complete except Listen Only (1) Basic Listener (2) Unaddress if MTA
LE0	Extended Listener	None
SR1	Service Request	Complete Capability
RL1	Remote/Local	Complete Capability (1) REN - Remote Enable (2) LLO - Local Lockout (3) GTL - Go to Local
PP0	Parallel Poll	No Capability
DC1	Device Clear	Complete Capability (1) DCL - Device Clear (2) SDC - Selected Device Clear
DT1	Device Trigger	Complete Capability GET - Group Execute Trigger
C0	Controller	No Capability
E1	Open Collector Bus Drivers	

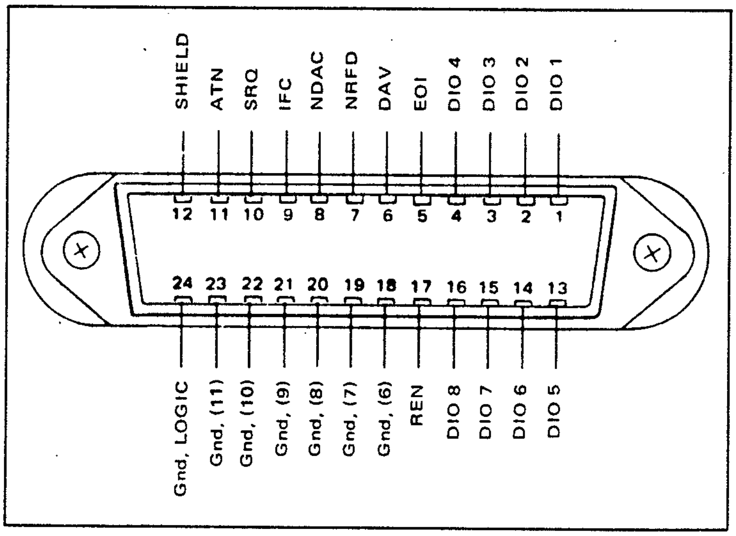


Figure 3.15 - GPIB Connector (Rear Panel)

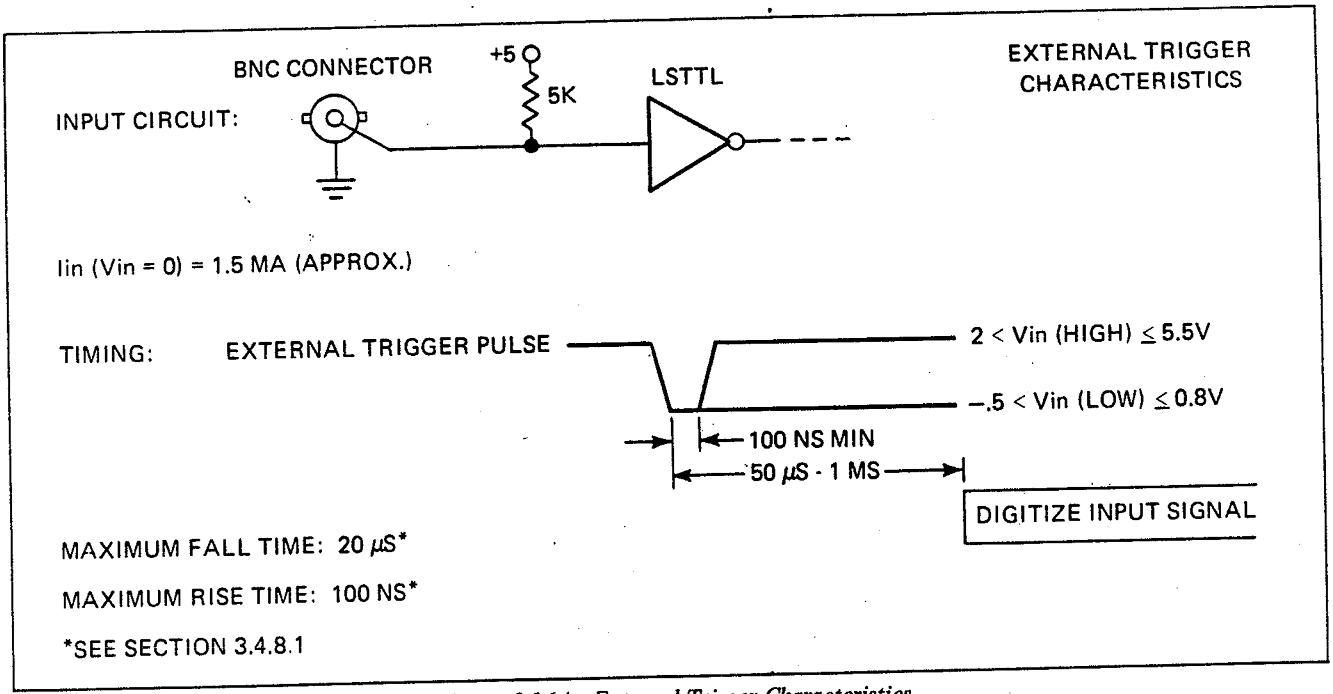


Figure 3.16A - External Trigger Characteristics

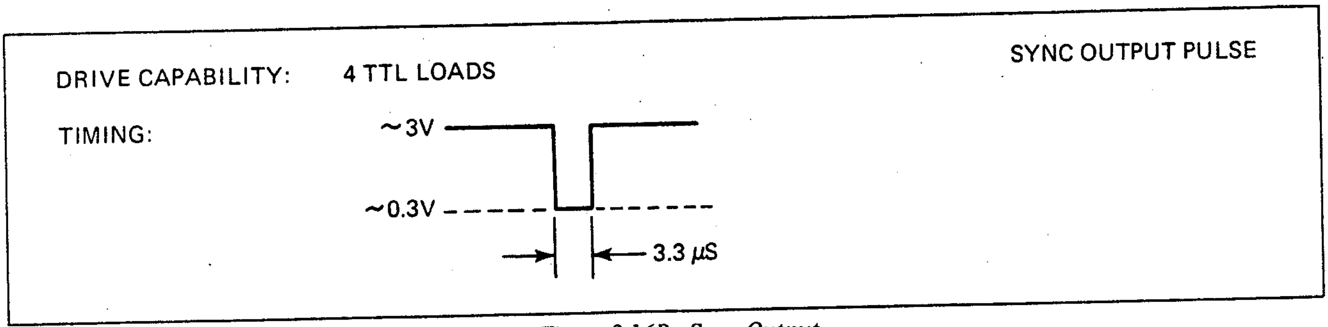


Figure 3.16B - Sync Output

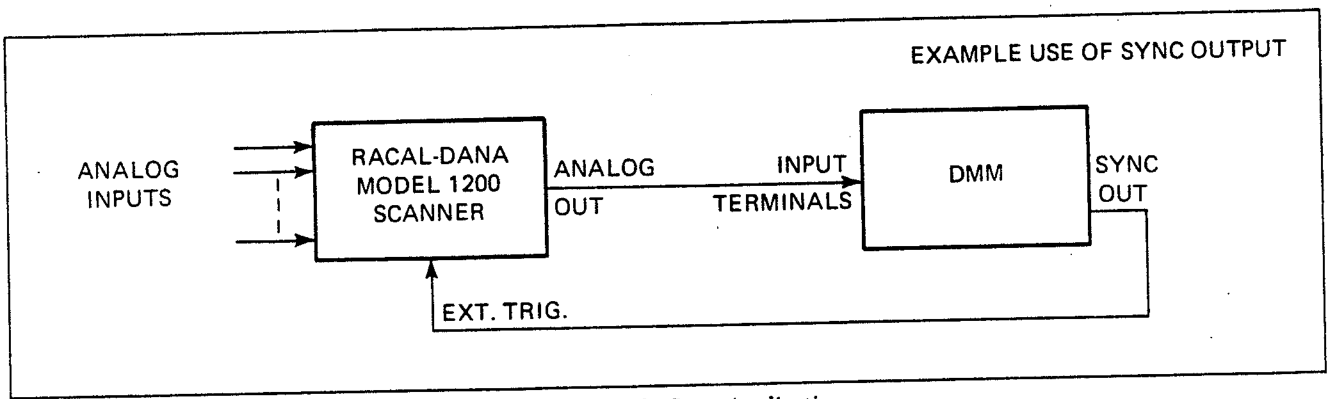


Figure 3.16C - Sync Application

3.5.3 GPIB Description.

3.5.3.1 Of the twenty-four lines available at the connector (shown in Figure 3.15) seven are grounds, one is a shield, and the remaining 16 lines are the signal lines. All of the signal lines are either input or output lines and have the following characteristics:

Logic Levels:	(1 = Low = ≤ .8V) (0 = Hi = ≥ 2.0V)
Input Loading:	Each input ~ two TTL loads
Output:	The output is capable of driving 15 interface bus loads. It consists of an open collector driver and is capable of sinking 48 mA with a maximum voltage drop of 0.5 volts. See IEEE-488 Electrical Specifications.

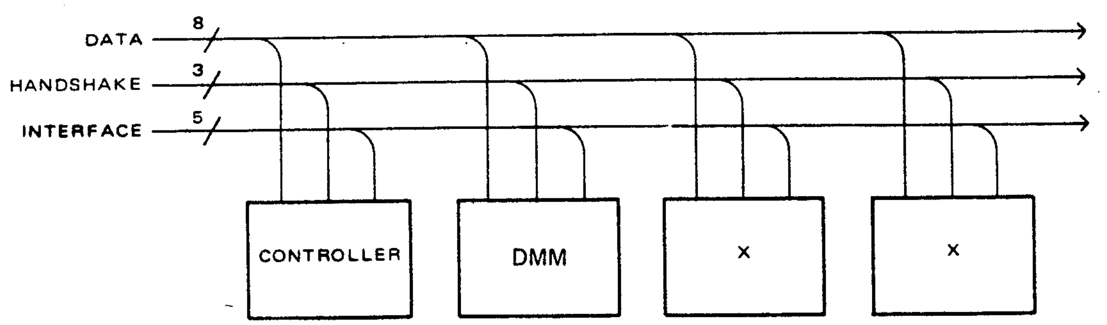
3.5.3.2 The signal lines, as shown in Figure 3.17 consist of three functionally separate sets: Data, Handshake and Interface.

3.5.3.3 DATA.

3.5.3.3.1 The data lines consist of lines DIO-1 through DIO-8. These lines are the lines over which data flows between all instruments on the bus in bit parallel, byte serial form.

3.5.3.4 HANDSHAKE.

3.5.3.4.1 The transfer lines consist of: DAV (data valid), NDAC (not data accepted), and NRFD (not ready for data). These lines provide communication (between the instrument that is talking and the instruments that are listening) to



PIN			PIN	
1	DIO-1 Data In/Out Bit 1 (LSB)	DATA LINES ARE USED TO TRANSFER DATA FROM ONE INSTRUMENT TO ANOTHER	12	SHIELD
2	DIO-2 Data In/Out Bit 2		18	GND
3	DIO-3 Data In/Out Bit 3		19	GND
4	DIO-4 Data In/Out Bit 4		20	GND
13	DIO-5 Data In/Out Bit 5		21	GND
14	DIO-6 Date In/Out Bit 6		22	GND
15	DIO-7 Data In/Out Bit 7		23	GND
16	DIO-8 Data In/Out Bit 8		24	LOGIC GND
6	DAV (DATA VALID)	HANDSHAKE LINES OPERATE IN A PROPER TIME SEQUENCE FOR COMPLETE COMMUNICATION BETWEEN INSTRUMENTS	25	NOT USED
7	NRFD (NOT READY FOR DATA)			
8	NDAC (NOT DATA ACCEPTED)			
5	EOI (END OR IDENTIFY)	INTERFACE LINES ARE USED TO PROVIDE AN ORDERLY FLOW OF INFORMATION BETWEEN UNITS		
9	IFC (INTERFACE CLEAR)			
10	SRQ (SERVICE REQUEST)			
11	ATN (ATTENTION)			
17	REN (REMOTE ENABLE)			

Figure 3.17 - Interface Signal Pin Assignments

synchronize the flow of information across the eight data lines. These lines derive their nomenclature from their meaning in the low or one state (eg: when NRFD is low the device is Not Ready For Data).

a. DAV. Signifies that valid information is available on the data lines.

b. NRFD. Signifies that the instrument is not ready to accept information.

c. NDAC. Signifies that the information is not accepted by the acceptor.

3.5.3.5 INTERFACE.

3.5.3.5.1 The five interface lines coordinate the flow of information on the bus.

a. Interface Clear
'IFC'. Places the DMM interface in the IDLE state. (Untalk, Unlisten).

b. Attention
'ATN'. Indicates the nature of information on data lines during a handshake transfer sequence. Low indicates data lines carry interface commands; high indicates that the data lines carry data.

c. Remote Enable
'REN'. Arms instrument to select Remote Operation. (Low for Remote)

d. Service Request
'SRQ'. Service request signal line. Signals the controller that a peripheral or bus member wants attention for such purposes as transmitting measurement, status or condition information to the bus controller.

e. End or Identify
'EOI'. End or Identify signal. Used for two purposes: (1) to signify the end of a message and (2) to signal bus peripherals to set the I/O bit assigned for parallel poll identification process.

3.5.4 GPIB Bus Structure.

3.5.4.1 The bus structure, to maintain an orderly transfer of data between the controller and devices, requires eight signal lines. Three signal lines (DAV, NRFD, and NDAC) to regulate transfers control are referred to as handshaking. Five signal lines (EOI, IFC, SRQ, ATN, and REN) to handle interface management are necessary to maintain a bi-directional data follow. The data lines D101 through D108 carry the bit parallel byte serial information between the talker and listener. Figures 3.17 and 3.18 illustrate the sequential relationship between DAV, NRFD and NDAC lines.

3.5.5 Address Assignment.

3.5.5.1 When the DMM is used as a system instrument it must be assigned an address as a bus member. The instrument is equipped with an address switch located on the rear panel which enables the user to assign it one of 31 decimal addresses. The decimal addresses available are the numbers 00 through 30.

3.5.5.2 Table 3.8 contains all of the information required for setting the instrument address switch and for determining the talk and listen address codes used in programming the controller.

3.5.5.3 Refer to Table 3.8 and note that the right hand column shows the decimal addresses available for assignment to the DMM. The column titled Address Switch Setting illustrates the positions of the switches for each decimal address. To set the address on the instrument at the desired decimal address, refer to Table 3.8, and set the switches on the address switch to the pattern shown in the Address Switch column of the table.

3.5.5.4 As an aid in setting the address switches, the decimal address may be displayed on the DMM readout by holding the "Local" key down. The address switches may then be set until the desired address appears on the display. Turning on the "Talk Only" switch will cause the displayed address to be 64 or greater. This illegal address is displayed to alert the user that the DMM is in the "talk only mode".

3.5.5.5 Once the instrument has been assigned an address, and the address switch has been set, the controller may address the instrument as a talker or as a listener by transmitting the appropriate ASCII character on the data lines. The Data Lines column shows the 7 bit binary code required for each talk and listen address assigned to the instrument. These are the codes the controller must transmit to establish the talker/listener condition of the DMM. Note that there are two address codes used for each decimal address. Each of these address codes constitutes a different ASCII character. For example, if it is desired to use the decimal address 02, the address switch on the rear panel of the instrument is set to the pattern shown in Table 3.8. As shown in the table, the talk address is the ASCII character " and the listen address is the ASCII character B. Note that the only difference in the binary code in each case is the state of data lines D6 and D7.

3.5.5.6 Table 3.8 illustrates the data line code in binary form for each decimal address. Again, using the example for decimal address 02, note that bits D1 through D5 are the same for both talk and listen address and that the only difference is in bits D6 and D7.

3.5.6 Bus Operation Sequence.

3.5.6.1 The transmission of programming instructions to the DMM and the subsequent transmission of measurement data to the controller are accomplished by transmitting programming instructions as outlined in the bus operation sequence in Table 3.9. Table 3.9 and the accompanying timing chart (Figure 3.19) illustrate the sequence of the transmission of device dependent messages to the DMM which cause it to measure the voltage applied to the input and then transmit the resultant measurement data to the controller via the interface bus.

3.5.6.2 Note that the left hand column of Table 3.9 contains line numbers. These are used for reference purposes throughout the following description of the bus operation sequence. The column titled Handshake Lines indicates the high/low condition of the handshake lines at various points throughout the two-way transmission of information. In a similar fashion the columns titled Interface Lines and Data Lines contain entries reflecting the state of the interface lines and data lines during operation. The column titled Meaning or Function contains entries explaining the purpose of each operational step during the data transfer.

3.5.6.3 A timing chart is included to illustrate the condition of each individual bus line at each stage of the data transfer operation. Note that the timing chart includes numbers adjacent to each level change. These numbers refer to the individual line entries of the table.

3.5.6.4 The measurement operation used in Table 3.9 is a simple voltage measurement. The measurement parameters are as follows: Function DC volts, Range 10 volts, Trigger continuous. Note that the measurement parameters are shown in the meaning or function column of the table in lines 17 through 22 and that the program string required to perform this measurement is F1R5T1. The program string will include a carriage return and line feed, but in this case this command is automatically transmitted by the Hewlett Packard 9825.

3.5.6.5 For purposes of this example it is assumed that the DMM has been assigned the decimal address 02 and that the controller is a Hewlett Packard 9825 calculator with a talk address U. It is further assumed that both the controller and the DMM are system connected, turned on and operational.

3.5.6.6 Table 3.9 shows the sequence of bus operation. Lines 1 through 13 show the detailed operation of the bus for one handshake cycle (ie: the transmission of one ASCII character as a bus message). Lines 14 through 44 do not indicate the detail for each handshake cycle; they indicate only the transmission of the characters required for the programming commands and the subsequent transmission of the data by the DMM. Each transmission by the controller or the DMM, shown in lines 14 through 44, requires the handshake cycle illustrated by line entries 1 through 13 of the table.

3.5.6.7 Refer to Table 3.9, line 1, and note that the first operation performed is the setting of the Remote Enable (REN) line to the low state. As explained in the table, this operation arms the bus members to go to the remote mode. The controller then transmits the interface clear (IFC) signal which stops bus activity and the attention (ATN) line is set low indicating that the next data byte placed on the bus by the controller will be a Bus Message. Note in the timing chart that when the ATN line is set low (3) that the DMM responds by setting the NRFD line high (4). This response by the DMM indicates that it is now ready to accept data.

3.5.6.8 When the DMM transmits the ready for data signal by setting the NRFD line high (line 4 of Table 3.9) the controller puts the bus message UNL on the data lines. As shown in line 5 of the table this is the ASCII character ?. The unlisten message is a universal message understood by all bus members as the command "unlisten". Having placed the data character on the lines, the controller now says the data is valid by setting the DAV line low (6). The DMM then says "I'm going to accept the data now on the data lines; don't change the data lines". The DMM then reads the data lines (8) and acknowledges acceptance of the data by setting the NDAC line high (9). The controller then removes the data valid signal (10), removes or changes data (11) and the DMM removes the data accepted signal from the bus (12).

3.5.6.9 At this point, one ASCII character has been transmitted by the controller to the DMM and the DMM is now ready to accept a new data byte. It indicates this (13) by setting the NRFD line high. The controller now puts the next character on the data line and the handshake cycle for the transfer of the character is repeated. The next character transmitted by the controller is the ASCII character U which is the talk address of the Hewlett-Packard 9825 calculator. As indicated in Table 3.9, by transmitting this character the calculator is making itself a talker. The next character transmitted is the quotation mark which is the listen address of the DMM when it has been assigned the decimal address 02.

3.5.6.10 Lines 16 through 24 of the table illustrate the sequence of transmission of the program string which instructs the DMM to make the DC voltage measurement. Lines 26 and 29 of the table indicate the end of transmission with the characters CR (carriage return) and LF (line feed). Note that at line 16 of the table the controller sets the ATN line high indicating that the program string to follow in lines 17 through 24 are device dependent messages.

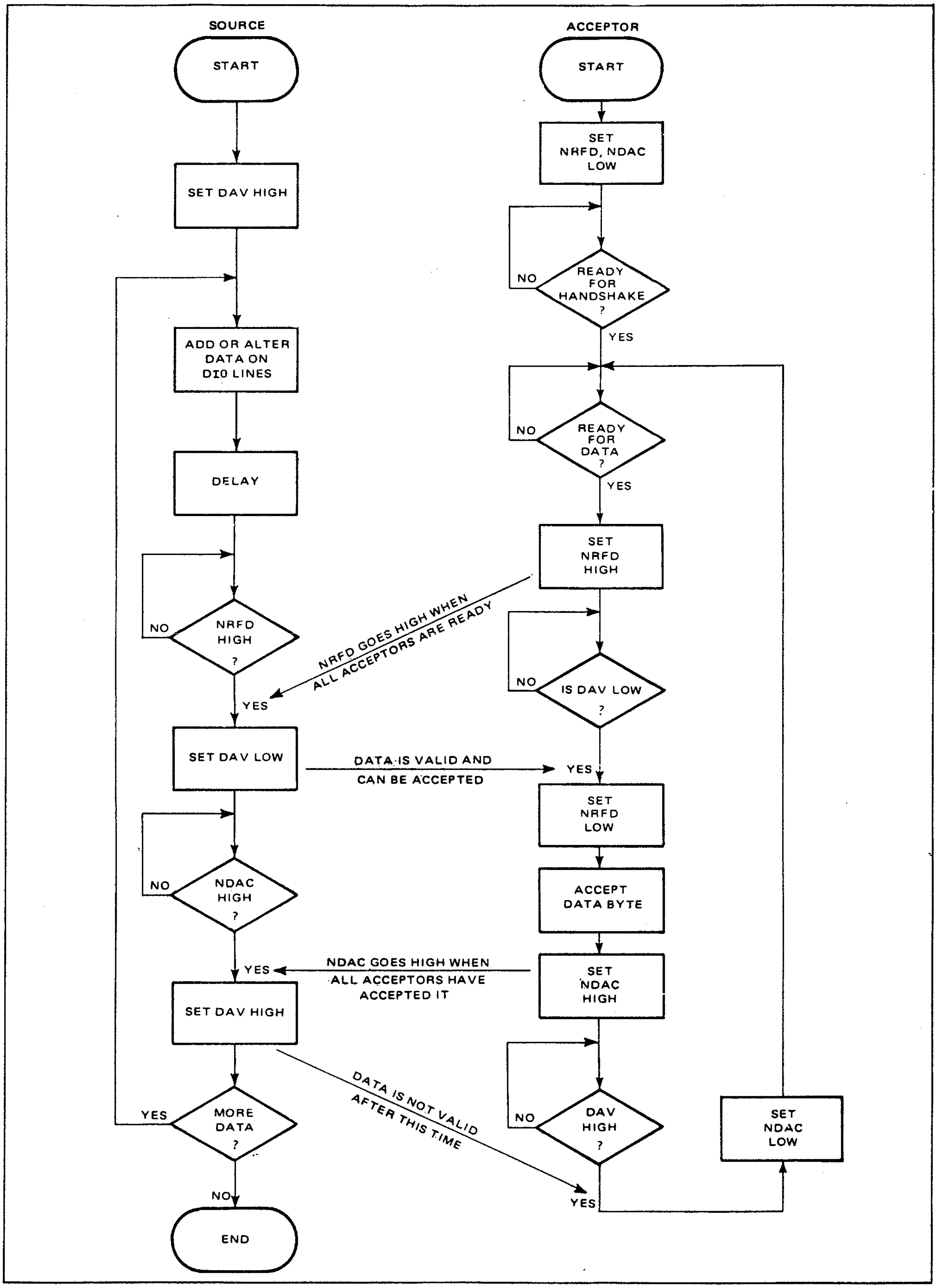
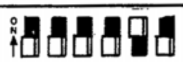
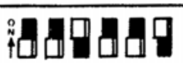
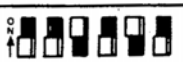
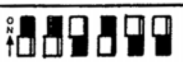
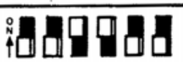
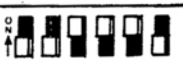


Figure 3.18 - Handshake Flow Chart

Table 3.8 - Instrument Address Selector

ASCII CHARACTERS		DATA LINES D_7	D_6	D_5	D_4	D_3	D_2	D_1	ADDRESS SWITCH SETTING	DECIMAL ADDRESS
TALK	LISTEN	TALK	LISTEN	ADDRESS 16	8	4	2	1	TALK ONLY A 5 4 3 2 1 	
	SP	0	1	0	0	0	0	0		00
@		1	0	0	0	0	0	0		
	!	0	1	0	0	0	0	1		01
A		1	0	0	0	0	0	1		
	"	0	1	0	0	0	1	0		02
B		1	0	0	0	0	1	0		
	#	0	1	0	0	0	1	1		03
C		1	0	0	0	0	1	1		
	$	0	1	0	0	1	0	0		04
D		1	0	0	0	1	0	0		
	%	0	1	0	0	1	0	1		05
E		1	0	0	0	1	0	1		
	&	0	1	0	0	1	1	0		06
F		1	0	0	0	1	1	0		
	' (APOSTROPHE)	0	1	0	0	1	1	1		07
G		1	0	0	0	1	1	1		
	(	0	1	0	1	0	0	0		08
H		1	0	0	1	0	0	0		
	)	0	1	0	1	0	0	1		09
I		1	0	0	1	0	0	1		
	*	0	1	0	1	0	1	0		10
J		1	0	0	1	0	1	0		
	+	0	1	0	1	0	1	1		11
K		1	0	0	1	0	1	1		
	,	0	1	0	1	1	0	0		12
L		1	0	0	1	1	0	0		
	–	0	1	0	1	1	0	1		13
M		1	0	0	1	1	0	1		
	.	0	1	0	1	1	1	0		14
N		1	0	0	1	1	1	0		
	/	0	1	0	1	1	1	1		15
O		1	0	0	1	1	1	1		

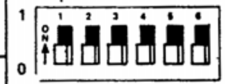
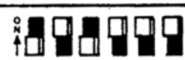
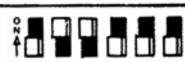
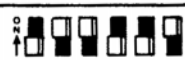
ASCII CHARACTERS		DATA LINES D_7	D_6	D_5	D_4	D_3	D_2	D_1	ADDRESS SWITCH SETTING	DECIMAL ADDRESS
TALK	LISTEN	TALK	LISTEN	ADDRESS 16	8	4	2	1	TALK ONLY A 5 4 3 2 1 	
	Ø	0	1	1	0	0	0	0		16
P		1	0	1	0	0	0	0		
	1	0	1	1	0	0	0	1		17
Q		1	0	1	0	0	0	1		
	2	0	1	1	0	0	1	0		18
R		1	0	1	0	0	1	0		
	3	0	1	1	0	0	1	1		19
S		1	0	1	0	0	1	1		
	4	0	1	1	0	1	0	0		20
T		1	0	1	0	1	0	0		
	5	0	1	1	0	1	0	1		21
U		1	0	1	0	1	0	1		
	6	0	1	1	0	1	1	0		22
V		1	0	1	0	1	1	0		
	7	0	1	1	0	1	1	1		23
W		1	0	1	0	1	1	1		
	8	0	1	1	1	0	0	0		24
X		1	0	1	1	0	0	0		
	9	0	1	1	1	0	0	1		25
Y		1	0	1	1	0	0	1		
	:	0	1	1	1	0	1	0		26
Z		1	0	1	1	0	1	0		
	;	0	1	1	1	0	1	1		27
[		1	0	1	1	0	1	1		
	<	0	1	1	1	1	0	0		28
\		1	0	1	1	1	0	0		
	=	0	1	1	1	1	0	1		29
]		1	0	1	1	1	0	1		
	>	0	1	1	1	1	1	0		30
^		1	0	1	1	1	1	0		
NONE		ILLEGAL							NONE	31

Table 3.9 - Bus Operation Sequence

	HANDSHAKE LINES	BUS LINES	DATA LINES	MEANING OR FUNCTION
1		REN Lo		Arms bus peripherals to go to remote mode.
2		IFC		Stops activity on the bus.
3		ATN Lo		Signifies that data byte will be a "Bus Message".
4	NRFD Hi			DMM says ready for data.
5			?	UNL (Unlisten) message (ASCII character ?) on data bus by controller means "all bus peripherals unlisten".
6	DAV Lo			Controller says data on bus is valid.
7	NRFD Lo			DMM says its not ready for new data; do not change data lines while DMM is accepting data.
8				DMM reads data lines.
9	NDAC Hi			DMM says it has read data.
10	DAV Hi		?	Controller says data no longer valid.
11	NDAC Lo			DMM removes data accepted flag.
12	NRFD Hi			DMM says it's ready for next data byte.
13				Controller removes or changes data on bus.
14			U	"I talk", controller becomes talker (HP9825 talker address).
15			"	"You listen", addressed peripheral becomes listener (In this case it is the DMM set to decimal address 02; see table 3.9).
16		ATN Hi		Signifies that data byte will be a "Device Dependent Message" as opposed to an "Interface Message".
17			F	Function
18			1	DC Volts
19			R	Range
20			5	10 Volts
21			T	Trigger
22			1	Continuous
23			CR	End of transmission by HP9825.
24			LF	
25		ATN Lo		Byte to follow is a Bus Message.
26			?	UNL (unlisten) bus message.
27			B	"You talk", DMM talk address (02).
28			5	"I listen", HP9825 listen address.
29		ATN Hi		Message to be transmitted by DVM is Data.
30			+	Measurement data transmitted by DMM
31			1	
32			•	
33			0	
34			2	
35			5	
36			4	
37			6	
38			E	Exponent Indicator means X 10^{01}
39			+	Sign of exponent.
40			0	Exponent. Here it indicates 10^{10}
41			1	
42			CR	End of data message.
43			LF	

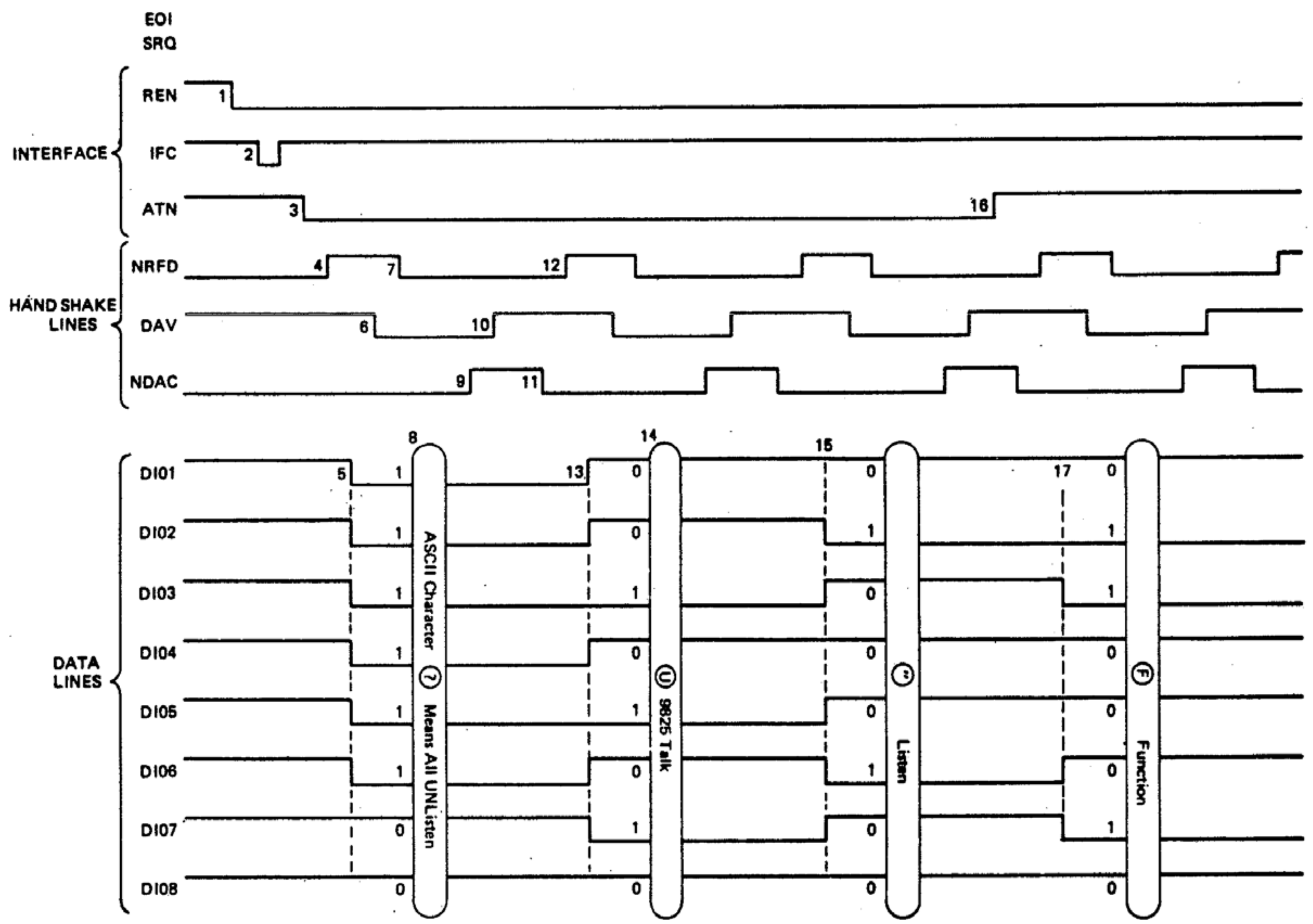


Figure 3.19 - Interface Timing

3.5.6.11 Having transmitted the program string of device dependent messages to the DMM, the controller then sets the ATN line low which indicates that the characters to follow in lines 26 through 28 are bus messages. These bus messages change the talker/listener relationship of the controller and DMM; the DMM is made a talker and the controller becomes a listener.

3.5.6.12 Lines 30 through 43 illustrate the sequence of the transmission of data by the DMM. The handshake sequence is the same when the DMM is transmitting data as that outlined in lines 1 through 13 of the table, except that the DMM is controlling the handshake lines.

3.5.6.13 Upon completion of the data transmission, the DMM transmits a carriage return (CR) and line feed (LF) to indicate the end of the data transmission. Refer to Table 3.10 for the GPIB programming requirements.

Table 3.10 - GPIB Programming Requirements

1. Character Code: 7 bit ASCII, upper or lower case.
2. All program strings transmitted to the DMM should end in a terminating character. Acceptable terminators are:
   - A. CR - Carriage Return
   - B. LF - Line Feed
   - C. EOI - This GPIB message EOI, true during transfer of the last byte of a string.
   - D. X - ASCII letter.
3. Programming numerical constant over the GPIB
   The following units are assumed when programming numerical constants over the GPIB:
   Volts
   Kohms,
   Hours • Minutes Seconds

3.5.7 Interface Message Repertoire.

3.5.7.1 The DMM is equipped with a standard GPIB interface which conforms to the specifications contained in IEEE-488-1978. The specification includes the definition of multi-line interface messages and this definition divides the messages into two groups; the primary command group and the secondary command group. The DMM includes none of the secondary command group in its interface message repertoire.

3.5.7.2 The primary command group of interface messages is further broken down into four lower categories: (1) the listen address group, (2) the talk address group, (3) the universal command group and (4) the addressed command group. The DMM is designed to include in its interface message repertoire 31 listen addresses and 31 talk addresses. The listen and talk addresses to which the DMM may be set are listed in Table 3.8.

3.5.7.3 The interface messages to which the DMM is designed to respond are listed in Table 3.11 along with their decimal equivalents, hex equivalents, meanings and data line codes. The function of the DMM in response to each of these commands is described in the following paragraphs.

3.5.7.4 GO TO LOCAL (GTL).

3.5.7.4.1 As shown in Table 3.11, the GTL command means go to local and the decimal and hex equivalent are both 01. Upon receipt of this interface message, the DMM, if previously programmed for remote, will return to its local operational state. This means that the instrument will then perform the function according to the settings of the front panel controls on the instrument until such time as it returns to remote control.

3.5.7.5 SELECTED DEVICE CLEAR (SDC).

3.5.7.5.1 Upon receipt of the SDC command, the DMM will go to the home state. The decimal and hex equivalent are both 04. The SDC message has the same effect as transmitting the GPIB program code 'Z' to the DMM.

3.5.7.6 GROUP EXECUTE TRIGGER (GET).

3.5.7.6.1 As shown in Table 3.11, the decimal and hex equivalents of the GET command are both 08. Upon receipt of the GET interface message, the DMM will trigger a reading if it had previously been placed in the HOLD mode. The group execute trigger command is used to trigger the simultaneous execution of a number of functions by a number of bus members at the same time. To use this command, one or more bus members are programmed to perform a function on receiving the GET interface message. Subsequently, the controller will transmit the GET command and all bus members previously programmed will begin execution on receipt of the command.

3.5.7.7 LOCAL LOCK OUT (LLO).

3.5.7.7.1 The DMM may be brought back into local control by pressing the "Local" key on the keyboard. If, however, the DMM receives an LLO (Hex 11 or decimal 17) command while in remote operation, it may not be brought back into local control through keyboard operation.

3.5.7.8 DEVICE CLEAR (DCL).

3.5.7.8.1 The decimal equivalent of the DCL command (as shown in Table 3.11) is 20, and the hex equivalent is 14. This command is identical in operation to the SDC command except that the DMM need not be a listener in order to respond to DCL. When this command is transmitted on the bus, all devices on the bus which respond to the DCL will clear. The DCL message has the same effect on the 5005 as transmitting the GPIB program code 'Z'.

3.5.7.9 SERIAL POLL ENABLE (SPE).

3.5.7.9.1 As shown in Table 3.11, the decimal equivalent of this interface command is 24; the hex equivalent is 18. The function of this command is to notify all bus members that they should output their serial poll status if made into a talker. Thus, when a bus member has transmitted a service request (SRQ), the bus controller can transmit the serial poll enable command, command each bus member to transmit its status byte by sequentially making each bus member a talker and thus identify the bus member requesting attention. Upon receipt of the DMM's talk address plus the SPE interface message, the DMM immediately prepares a status byte for transmission to the controller. If the DMM has previously transmitted an SRQ, it will set bit 7 of the status byte to 1. The serial poll allows a bus member to set the service request line to the 1 state, thus indicating to the controller that it wants attention. The controller may then sequentially interrogate each bus member to determine which one has requested service and the purpose of the request. The meanings of the bits in the status bytes are shown in Figure 3.20 and listed below:

a) Requested Service (DIO7). This bit indicates whether the DMM caused the SRQ (service request) line to be driven to the 'true' state; thus the controller can determine if the DMM is requesting service.

b) Abnormal Condition (DIO6). If true, this bit indicates the presence of an illegal or abnormal condition in the DMM, and is always in the same logical state as the DIO4 bit (see below).

c) Signal Integrate (DIO5). This bit is true during the time that the input (or external reference) signal is being measured by the DMM. In measurement systems where high throughput is important, this can be sampled by the controller to determine the earliest moment that the DMM's input signal can be changed, thus allowing multiple input signals to be measured in rapid succession. Note however that if the DMM is programmed to AUTO range, the Signal Integrate bit will go true multiple times as the DMM upranges or downranges.

d) Error Number Available (DIO4). This bit, which tracks bit DIO6 exactly, indicates that the DMM's Error Message register has been updated with a new error message. The error message can be retrieved

Table 3.11 - Interface Messages Used With The DMM

Message	Meaning	HEX CODE	Decimal Equiv.	DATA LINE CODE						
				7	6	5	4	3	2	1
GTL	Go To Local	01	1	0	0	0	0	0	0	1
SDC *	Selected Device Clear	04	4	0	0	0	0	1	0	0
GET *	Group Execute Trigger	08	8	0	0	0	1	0	0	0
LLO	Local Lock Out	11	17	0	0	1	0	0	0	1
DCL	Device Clear	14	20	0	0	1	0	1	0	0
SPE	Serial Poll Enable	18	24	0	0	1	1	0	0	0
SPD	Serial Poll Disable	19	25	0	0	1	1	0	0	1
UNL	Unlisten	3F	63	0	1	1	1	1	1	1
UNT	Untalk	5F	95	1	0	1	1	1	1	1

*Instrument will ignore message unless it is a listener over the bus by use of the 'Y' command which is described in Section 3.5.20.

e) Data Ready (DIO1). This bit is affected by the completion of a reading as well as the most recently programmed Interrupt Command (D0-D3). Section 3.5.22 gives more details on the Interrupt (D0-D3) commands.

3.5.7.10 SERIAL POLL DISABLE (SPD).

3.5.7.10.1 As shown in Table 3.11 the decimal equivalent to the SPD command is 25; the hex equivalent is 19. The function of this command is to return the bus members to their original states after the serial poll transaction has been completed.

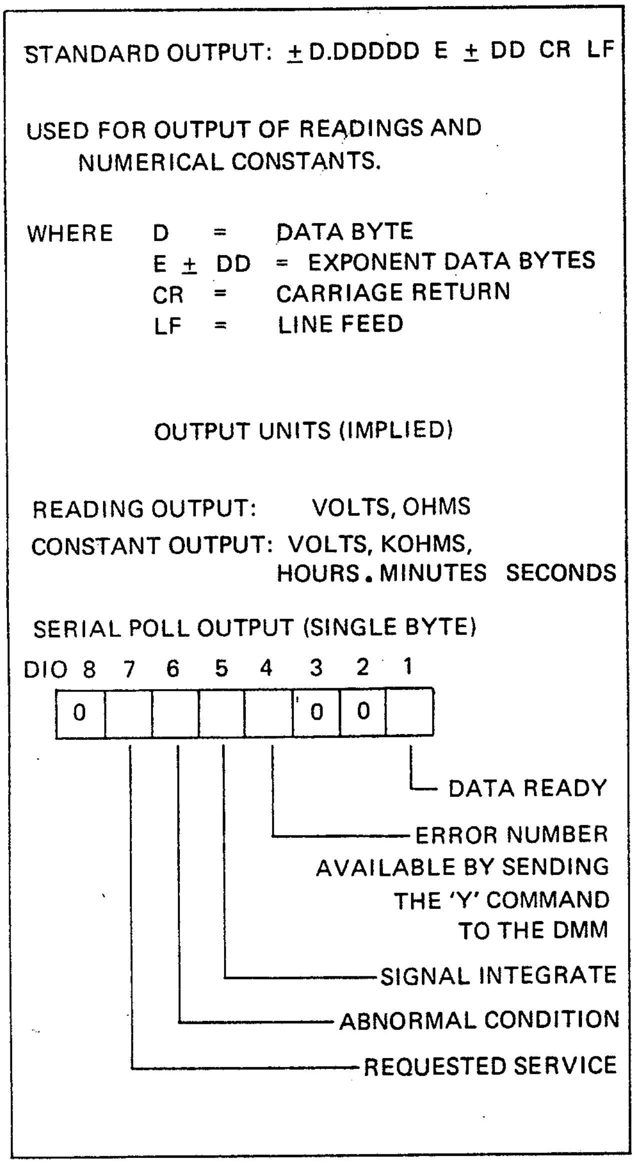


Figure 3.20 - GPIB Output Formats

3.5.7.11 UNLISTEN (UNL).

3.5.7.11.1 As shown in Table 3.11 the decimal equivalent of this command is 63; the hex equivalent is 3F. This command is also a universal interface message understood by all members of the bus as a command to go to the unlisten state. When this command is transmitted, all bus members previously in the listen state will return to the unlisten state.

3.5.8 Device Dependent Messages.

3.5.8.1 The messages which control the operation of the DMM when in system operation are referred to as device dependent messages. These messages listed in Table 3.12 are simply combinations of ASCII characters which the instrument recognizes as specific instructions. To program the instrument for a specific operation, the operator programs the controller to transmit a sequence of these messages (referred to as a program string). The program string is variable in length and has no fixed format. Individual commands may be transmitted in any order and require no delimiters or spacing for the instrument to understand. A terminator character(s) should be sent as the last character in each program string. Acceptable terminators are CR (Carriage Return), LF (Line Feed), the GPIB message EOI in conjunction with the last byte of the string, also ASCII x lower case or X uppercase, or any combination of these. Most controllers will add terminator to the program string automatically. Alphabetic characters may be either upper or lower case. Table 3.10 summarizes the GPIB programming requirements.

3.5.8.2 The device dependent messages are listed in Table 3.12 along with the DMM operation and any special notes that apply. The device dependent messages applicable to the DMM are divided into subcategories such as Function Commands and Range Commands. In general, the various commands cause the instrument to perform the same functions as the front panel controls. There are special cases however, where there are extra functions available under remote control which are not available in the bench operation mode. Further, there are some special situations requiring special attention to the operation sequence used with the DMM.

3.5.8.3 To assemble a program string, first list the requirements of the program, and then select the appropriate program codes from Table 3.12. Table 3.9 shows a program string listing for a typical measurement procedure.

3.5.9 GPIB STORE and RECALL Commands.

3.5.9.1 Two main buffers are used during GPIB STORE/RECALL Commands. These commands cause readings and numerical constants to be moved from one memory location to another inside the DMM. To understand how these commands operate, refer to Figure 3.21. The output buffer

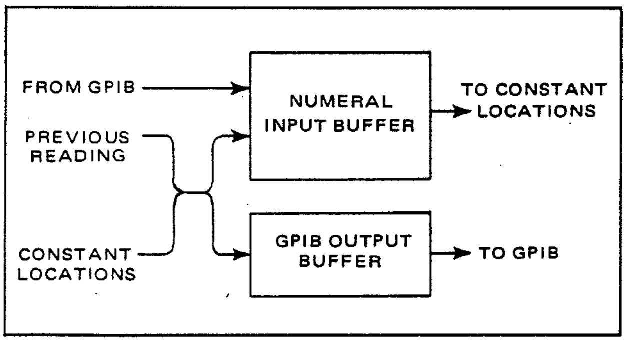


Figure 3.21 - GPIB Numerical Buffers

holds the ASCII characters which are waiting to be transmitted to the controller. The input buffer has two uses. During the entry of numerical constants from the bus, the input buffer is used as the holding register. Also, the input buffer is used to hold the number which was most recently transferred to the output buffer.

3.5.9.2 GPIB Store Commands cause the contents of the Numerical Input Buffer to be transferred to a constant location in the DMM's memory as follows:

a) N2, store as a NULL constant.

b) P2, store as a Percent constant.

c) L6, store as a LAH cycle constant, 'C'.

d) S2-S7, store as TIME constants.

Either the previous reading or a GPIB entered constant can be stored. For instance, if a reading is completed and then an N2 command is sent to the DMM, the reading will be stored as the NULL constant. If any of the following command strings are transmitted to the DMM:

–2.5e-3 N2

–2500000 E-9 N2

–000000000.0025 N2

–.000000000025E+08 N2

then –.0025 will be stored as the Null Constant.

3.5.9.3 GPIB RECALL Commands cause numerical constant(s) to be copied into the Numerical Input and GPIB Output Buffers for transmission to the controller as follows:

a) N3, transmit NULL Constant.

b) P3, transmit Percent Constant.

c) L7, transmit 5 LAH constants.

d) S8, transmit 6 TIME constants.

e) C1, transmit contents of Data Buffer.

3.5.9.4 The following points should be kept in mind when using GPIB recall commands:

a) The outputting of the above-mentioned data and constants takes priority over outputting of readings to the bus. In other words, readings will be displayed but not saved for GPIB output if the GPIB Output buffer is occupied by an out-going constant.

b) When the outputting of constant(s) is completed, the DMM will automatically resort to outputting readings.

c) Output Commands are not "stored" internally, therefore if more than one is sent, only the most recently transmitted output command will be honored.

3.5.9.5 The following apply only when outputting multiple constants (GPIB commands L7, S8, C1).

a) In keeping with the IEC and IEEE recommendations, multiple constants are separated by commas (,) and a terminator(s) CR LF appears after the last constant. This may require special programming on some controllers which do not meet IEC/IEEE recommendations.

b) As each constant is outputted, the DMM aborts any reading presently in progress and will re-start the reading. This may lower the read rate for a split second as the constants are output.

Table 3.12 - Model 5005/5006 Device Dependent Program Code

INITIALIZE COMMANDS

Operation	Program Code	Special Notes
Initialize	Z	Same as G0T1N0P0L0S0

FUNCTION COMMANDS

Operation	Program Code	Special Notes
DC Volts	F1	
AC Volts	F2	
Ohms	F3	
Ohms	F4	

RANGE COMMANDS

Operation	Program Code	Special Notes
AUTO Range	R0	
.1V, .1KΩ	R3	
1V, 1KΩ	R4	
10V, 10KΩ	R5	
100V, 100KΩ	R6	
1000V, 1000KΩ	R7	
10,000KΩ	R8	

TRIGGER COMMANDS

Operation	Program Code	Special Notes
Trigger Immediate	T0	Normally used in conjunction with T3.
Internal Trigger	T1	Causes continuous readings.
External Trigger	T2	Waits for trigger from rear panel BNC.
Hold/Manual	T3	Waits for trigger from GPIB or from keyboard.
External Trigger with Timeouts	T4	Same as T_2 and T_3, except that an internal time delay is inserted to allow for analog settling times.
Hold/Manual with Timeouts	T5	

Table 3.12 - Model 5005/5006 Device Dependent Program Code continued

LOW/HIGH RESOLUTION COMMANDS

Operation	Program Code	Special Notes
4 1/2 digit display	I1	
5 1/2 digit display	I2 I3	

FILTER COMMANDS

Operation	Program Code	Special Notes
Filter Out	J0	
Filter In	J1	Selects the 3-pole active filter.

INTERRUPT COMMANDS

Operation	Program Code	Special Notes
No SRQ when Reading is Ready	D0	
SRQ when Reading is Ready	D1	
SRQ if Reading* is < 0	D2	
SRQ if Reading* is ≥ 0	D3	

*Reading after being modified by Null, % and LAH.

SIGNAL/REFERENCE INPUT COMMANDS

Operation	Program Code	Special Notes
Signal Input	V0	Measurements taken from the signal input terminals.
Reference Input	V1	Measurements taken from the Reference input terminals.

Table 3.12 - Model 5005/5006 Device Dependent Program Code continued

COMMAND STRING TERMINATOR (OPTIONAL)

Operation	Code	Special Notes
Terminator	X	Use is required only when the DMM is being programmed from a controller which does not terminate the program string with a CR, LF, or EOI.

ERROR OUTPUT COMMAND

Operation	Program Code	Special Notes
Error Output	Y	Output most recent error number.

DIGITAL ZERO COMMAND

Operation	Program Code	Special Notes
Ignored	K0	
Ignored	K1	
Zero Command	K2	DC Function 0.1V range (F1R3), must have been previously selected, and a short must be supplied across the input terminals.

CALIBRATION COMMANDS

Operation	Program Code	Special Notes
Decrease offset, this range	K3	These commands have no effect unless the front panel calibration button is depressed, or shorted as described in maintenance section 5.1.6.
Nominal offset, this range	K4	
Increase offset, this range	K5	
Decrease scale, this range	K6	
Nominal scale, this range	K7	
Increase scale, this range	K8	
Calculate and Store Checksum	K9	

Table 3.12 - Model 5005/5006 Device Dependent Program Code continued

NULL COMMANDS

Operation	Program Code	Special Notes
Disable Null	N0	
Enable Null	N1	Subtracts null constant from reading.
Store as Null	N2	Stores previous reading or entered constant as null constant.
Transmit Null	N3	Output null constant to GPIB.

PERCENT COMMANDS

Operation	Program Code	Special Notes
Disable % equation	P0	
Enable % equation	P1	
Store as % constant	P2	
Transmit % constant	P3	

LOW AVG HIGH (LAH)

Operation	Program Code	Special Notes
Disable LAH	L0	
Enable and display/ output reading	L1	
Enable and display/ output Low	L2	
Enable and display/ output Avg	L3	
Enable and display/ output High	L4	
Enable and display/ output # rdgs so far	L5	
Store as number to be averaged	L6	
Transmit constants:	L7	Outputs to GPIB: Low, Avg, High, #rdgs (n), Average cycle constant (c)

Table 3.12 - Model 5005/5006 Device Dependent Program Code continued

PROGRAM BUFFER STORE COMMANDS

Operation	Program Code	Special Notes
Store to Pgm 0	A0	Store present machine setting to program buffer location 0.
Store to Pgm 1	A1	Store present machine setting to program buffer location 1.
Store to Pgm 2	A2	Store present machine setting to program buffer location 2.
Store to Pgm 3	A3	Store present machine setting to program buffer location 3.
Store to Pgm 4	A4	Store present machine setting to program buffer location 4.
Store to Pgm 5	A5	Store present machine setting to program buffer location 5.
Store to Pgm 6	A6	Store present machine setting to program buffer location 6.
Store to Pgm 7	A7	Store present machine setting to program buffer location 7.
Store to Pgm 8	A8	Store present machine setting to program buffer location 8.
Store to Pgm 9	A9	Store present machine setting to program buffer location 9.

PROGRAM BUFFER RECALL COMMANDS

Operation	Program Code	Special Notes
Recall Program 0	B0	Recall the machine setting previously stored at location 0.
Recall Program 1	B1	Recall the machine setting previously stored at location 1.
Recall Program 2	B2	Recall the machine setting previously stored at location 2.
Recall Program 3	B3	Recall the machine setting previously stored at location 3.
Recall Program 4	B4	Recall the machine setting previously stored at location 4.
Recall Program 5	B5	Recall the machine setting previously stored at location 5.
Recall Program 6	B6	Recall the machine setting previously stored at location 6.
Recall Program 7	B7	Recall the machine setting previously stored at location 7.
Recall Program 8	B8	Recall the machine setting previously stored at location 8.
Recall Program 9	B9	Recall the machine setting previously stored at location 9.

DATA BUFFER COMMANDS

Operation	Program Code	Special Notes
Clear Data Buffer	C0	
Output Contents of Data Buffer to the GPIB	C1	Outputs entire contents of data buffer

Table 3.12 - Model 5005/5006 Device Dependent Program Code continued

EXTERNAL REFERENCE FUNCTION COMMANDS (SOFTWARE RATIO)

Operation	Program Code	Special Notes
Internal Reference	G0	Disables Software Ratio.
DC Reference	G1	Enable Software Ratio.
AC Reference	G2	
Ohms Reference	G3	
Ohms Reference	G4	

EXTERNAL REFERENCE RANGE COMMANDS

Operation	Program Code	Special Notes
AUTO Range	Q0	Returning the DMM to internal reference will not affect the external reference range setting.
.1V, .1KΩ	Q3	
1V, 1KΩ	Q4	
10V, 10KΩ	Q5	
100V, 100KΩ	Q6	
1000V, 1000KΩ	Q7	
10000KΩ	Q8	

TIME

Operation	Program Code	Special Notes
Disable Time	S0	
Enable Time function	S1	DMM should be in HOLD mode (T3-Command) when TIME function is enabled.
Store as start Time	S2	
Store as stop Time	S3	
Store as interval	S4	
Store as subinterval	S5	
Store as N	S6	
Store as present Time	S7	
Output time constants to the GPIB	S8	Output Present time, N, Subinterval, Interval, Stop time, and Start time.

3.5.10 Initialize Command.

3.5.10.1 The program code 'Z' is normally used by the controller to place the DMM into a known state. This program code is equivalent to the following string: G0T1N0.

G0 - Internal reference
T1 - Internal trigger
N0 - Disable NULL
P0 - Disable percent
L0 - Disable LAH
S0 - Disable Time

3.5.11 Function Commands.

3.5.11.1 Function commands are available to program the instrument to perform any operation which may be commanded through use of front panel keyboard controls. Note that in Table 3.9 the DMM Operation column lists the functions available on the instrument and that the Program Code column shows the ASCII characters required to program the instrument for each of these functions. To program a function the controller need only transmit the ASCII characters required for the desired function (eg: to program the measurement function DC volts, the controller simply transmits the two ASCII characters F and 1 over the bus to the DMM).

3.5.12 Range Commands.

3.5.12.1 Seven individual range commands are available to the controller; one to command the autorange and six additional commands for selecting specific ranges for the instrument. Note that the commands R3 through R7 all serve dual purposes; they command ranges for voltage measurements and for resistance measurements.

3.5.13 Trigger.

3.5.13.1 Trigger commands T0 through T5 control the beginning of a measurement cycle. When the T1 command is transmitted, the instrument operates on the internal trigger on its normal measurement timing cycle (see Figure 3.22). When the T2 command is transmitted, the instrument must be triggered by an external signal inputted through a BNC connector on the rear panel of the instrument. When the T3 command is transmitted, the instrument is put in the "Hold" state and will stay there until it is triggered either from the front panel or from the GPIB. Trigger commands from the GPIB can be either a T0 command or a Group Execute Trigger. Trigger commands are given from the keyboard by pressing 'Track' or 'Single' when the DMM is in local control. Upon receipt of the T4 program code the instrument goes into the External trigger mode and must be triggered by an external signal connected to the rear panel BNC connector. After being triggered via the rear panel BNC, the DMM executes a timeout which allows time for analog signals to settle. The timeout will vary, depending upon which functions and ranges are selected, before triggering a single reading. When program code T5 is transmitted, the instrument goes into the "Hold" mode described above except that its measurement cycle is again affected by the timeouts applicable to each function and range. For a complete description of 'TIME-OUTS' see paragraph 3.6.

3.5.14 HI-LO Resolution Commands.

3.5.14.1 The measurement accuracy of the DMM is directly proportional to the signal integration time (ie: the longer the integration time, the more accurate the measurement). If the measurement time is available, more accuracy may be obtained by programming the longer integration period. In situations where speed is required, the shorter integration time may be programmed at some sacrifice in measurement accuracy. The program codes I1, I2 and I3 select the resolution, the accuracy and the reading rate. Code I1 enables the 4 1/2 digit display which generates higher speed at the sacrifice of accuracy. Codes I2 and I3 develop greater accuracy at reduced speed.

3.5.15 Null Commands.

3.4.15.1 Program codes N0 through N3 call for the Null functions. The N1 program code enables the Null function. Upon receipt of N1 from the interface, a flag is set in

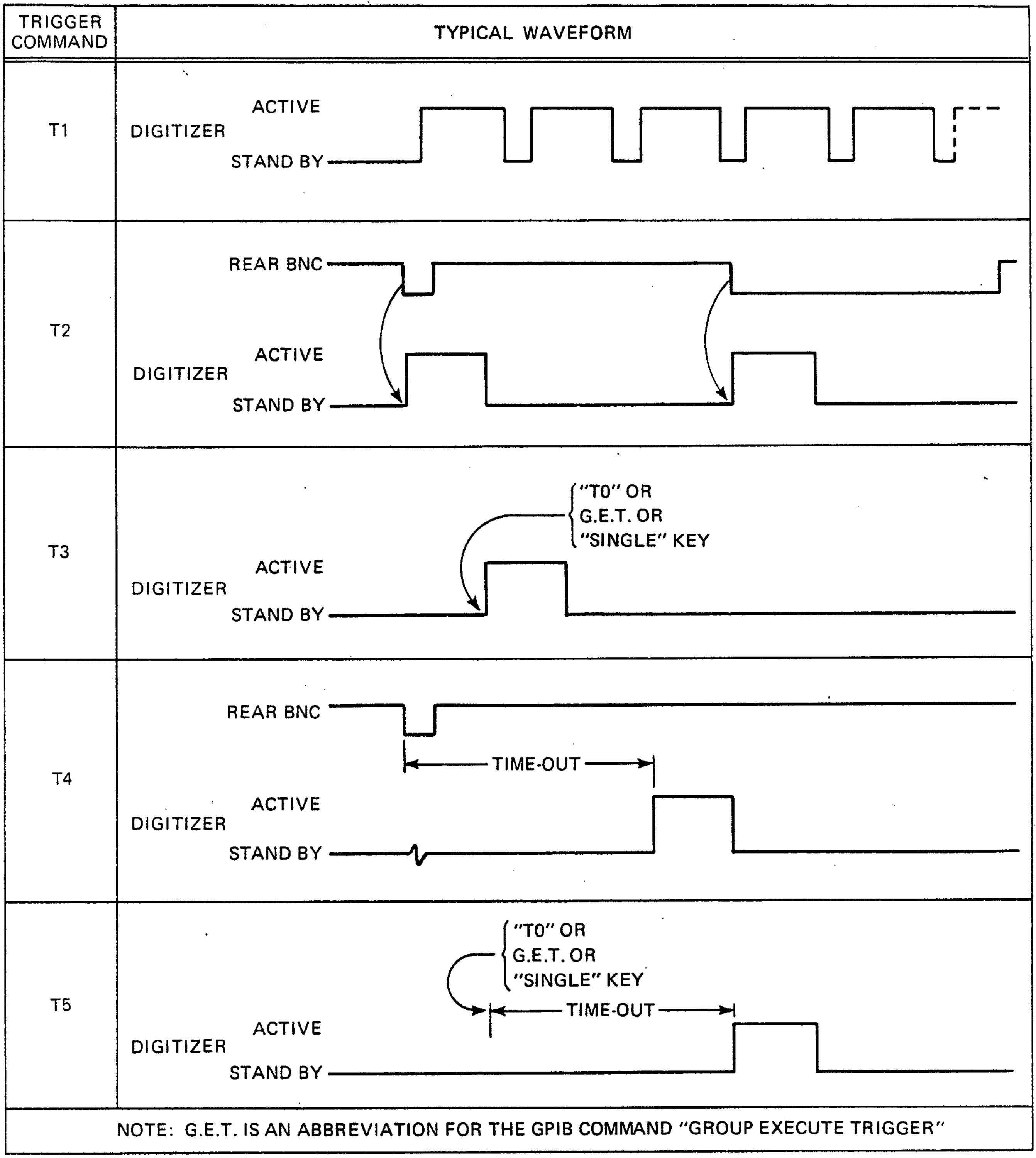


Figure 3.22 - Trigger Command Measurement Timing

memory which signals the Computer to subtract the Null constant from future readings. The N2 program code allows for the storage of Null constants. Upon receipt of the N2 command, the previous reading or a constant enter via the GPIB is stored into memory for use as the Null constant. The N3 program code causes the DMM to transmit the Null constant to the controller.

3.5.15.2 The N1N2 program string accomplishes the same operation as selection of the "Null" key on the keyboard. Program code N0 disables the Null function but does not change the Null constant.

3.5.16 Interrupt Commands.

3.5.16.1 Commands may be transmitted by the controller to instruct the DMM to send an SRQ (Service Request) signal over the GPIB. When the SRQ occurs, the controller can read the DMM's Serial Poll status byte to determine the cause of the SRQ. Figure 3.20 identifies the Data Ready bit in the status byte which will set to 1 if the SRQ was sent to inform the controller that a reading is ready for transmission over the bus.

3.5.16.2 The Interrupt Commands D0-D3 determine what type of readings will cause the SRQ and Data Ready messages to become true, as shown in Table 3.13 and explained below. If the D0 command is programmed, the DMM will not send an SRQ or set the Data Ready bit true when a reading becomes available for GPIB output. If the D1 command is programmed, the DMM will always send an SRQ and set the Data Ready bit in the status byte.

Table 3.13 - Effects of D0 Thru D3 Interrupt Commands

Most Recently Transmitted 'D' Command	Newly Completed DMM Reading (after Null, %, etc.)	Service Request SRQ	Serial Poll Status Byte	
			Requested Service Bit (DIO7)	Data Ready Bit (DIO1)
D0	+ or – polarity	False (1)	0 (2)	0
D1	+ or – polarity	True	1	1
D2	– polarity	True	1	1
	+ polarity	False (1)	0 (2)	0
D3	+ polarity	True	1	1
	– polarity	False (1)	0 (2)	0

(1) May be driven True by another bus member.

(2) Usually zero, but may be set to one for reason other than Data Ready.
See Section 3.5.7.9 for further explanation.

3.5.16.3 If the D2 command is programmed, an SRQ will be sent and the Data Ready bit will be set, but only if the reading (after Null, %, etc.) has a negative polarity sign (number is less than zero). If the D3 command is programmed, an SRQ will be sent and the Data Ready bit will be set, but only if the reading (after Null, %, etc.) has a positive polarity sign (number is greater than or equal to zero).

3.5.16.4 The D2 and D3 commands can be used to notify the controller that the DMM's input signal has increased or decreased across an important boundary. For instance, if +2.0 is programmed as the Null constant and Null is enabled, the D2 or D3 command can be used to notify the controller that the input signal has moved across +2 volts.

3.5.16.5 The following should be kept in mind when using the D1, D2 or D3 commands:

a) The SRQ line and Data Ready bits can be reset to their home state in the following ways:

  1) Both are reset whenever the DMM is reprogrammed over the bus.

  2) Both are reset by making the DMM a talker and accepting the entire reading from the DMM over the bus.

  e) SRQ will be reset whenever the controller reads the DMM's serial poll status byte.

b) If the DMM is programmed with the D2 or D3 command, the SRQ line and Data Ready bit will remain true even though the most recent reading may not be the proper polarity to cause them to be set true. For example, if the D2 command is programmed and then a negative reading followed by a positive reading is taken, the SRQ line and Data Ready bits will remain set, assuming of course, that none of the procedures listed in a) take place.

3.5.17 Filter Commands.

3.5.17.1 Control of the active filter in the remote mode is the same as manual control of the filter except that the controller transmits the program code commands J0 and J1 (as shown in Table 3.12).

3.5.18 Digital Zero Command.

3.5.18.1 The code F1R3 must precede the Digital Zero command code K2 to enable the Digital Zero command. Furthermore, the HI-LO INPUT terminals on the front or rear panel of the DMM must be shorted.

3.5.19 Command String Terminator.

3.5.19.1 The terminator code "X" permits the controller to terminate the program string when other terminating codes were not included in the string: typical terminators are CR, LF, or EOI. Most modern controllers will append a terminator to program strings automatically, making the use of 'X' program code unnecessary.

3.5.20 Error Output Command.

3.5.20.1 When a programming error or operational error is discovered by the DMM when in remote, an SRQ is sent to the controller. Upon receiving the SRQ, the controller should read the DMM's status byte to determine why the SRQ was sent. If the status byte contains '1' in the DIO-4 position (see Figure 3.20) then an error has occured and an error number can be transmitted to the controller. To obtain this error message number, the controller first sends the program code 'Y' (why) to the DMM and then reads the error message number from the DMM. Table 3.6 can then be used to determine the nature of the problem.

3.5.21 Calibration Commands.

3.5.21.1 If a CAL LAB is handling more than ten 5004 series voltmeters, it may be advantageous to automate the calibration of the DMM's. To do this, the front panel "CAL" switch on the main PCB is shorted and commands K3 through K8 are transmitted to the DMM to modify Non-Volatile memory constants. After all other Cal commands are completed, the K9 command should be transmitted to the DMM. When the calibration is completed, the short across the Cal switch *must* be removed. Additional details are presented in Section 5.3.4.

3.5.22 Signal/Reference Input Commands

3.5.22.1 The Signal/Reference input command is an Extended Software Capability feature of the DMM. This feature allows the External Reference Input Terminals to be utilized as an additional pair of signal input terminals when not used for ratio measurements.

3.5.22.2 Neither is this feature selectable from the keyboard nor are front panel LED annunciators provided to indicate which set of input terminals are presently selected.

3.5.22.3 Program code V0 selects the Signal input terminals for measurements and code. V1 selects the Reference input terminals. The following guidlines will be observed when using the V1 command:

a) Ohms measurements cannot be made through the Reference Input terminals.

b) The V1 command reverses the role of the Signal and Reference inputs during External Reference (Software Ratio) measurements. Further information is provided in Section 3.5.19.

3.5.23 Time Commands.

3.5.23.1 Program Codes S0 through S8 address the DMM real-time clock as it is applied to readings in progress. The Start Time, Stop Time, Time Interval, Subinterval Time and number of readings per interval can be selected and stored.

3.5.24 Percent Commands.

3.5.24.1 The Percent Commands of P0 and P3 can enable or disable the % equation $\left(\frac{\text{READING-REFERENCE}}{\text{REFERENCE}}\right) \text{X } 100$

which is the percentage deviation of the input reading from a reference value. Storing as a % constant or transmitting as a % constant completes this message group.

3.5.25 LOW-AVERAGE-HIGH Commands (LAH).

3.5.25.1 The program codes L0 through L7 can disable or enable the LAH function or execute the LAH modes which are described in section 3.4.8.They store the number to be averaged or Transmit the LAH constants included in this group of device dependent messages.

3.5.26 Program Buffer Store Commands.

3.5.26.1 Up to 10 instruments settings can be stored with the program codes A0 through A9. Each code stores to one program number. The detail operation of the Program Buffer is presented in section 3.4.12.2.

3.5.27 Program Buffer Recall Commands.

3.5.27.1 The 10 instrument settings can be recalled with the program codes B0 through B9. The setting stored to a program number can be recalled in any sequence. The operation of the recall function of the program buffer is presented in section 3.4.12.2.

3.5.28 Data Buffer Commands.

3.5.28.1 The two program codes for Data Buffer can address the two buffer modes which are:

a) Clear the Data Buffer.

b) Recall previous readings from the Data Buffer to the GPIB. (See also section 3.5.9)

Table 3.14 - Signal/Reference and Software Ratio Codes

Most Recent GPIB Program Code	Signal Input Terminals	Ext. Ref Input Terminals*	Ratio Displayed
V0 (Signal Input terminals selected)	Measurement Signal	Reference Signal	Ratio = $\frac{\text{Signal Terminals}}{\text{Ext. Ref Terminals}}$
V1 (Ext. Ref. Input terminals selected)	Reference Signal	Measurement Signal	Ratio = $\frac{\text{Ext. Ref Terminals}}{\text{Signal Terminals}}$

*ohms measurements cannot be made through Ext. Reference Input Terminals

3.5.29 Software Ratio Commands (External Reference).

3.5.29.1 When in the Software Ratio mode, the DMM reads the External Reference Signal, then calculates:

$$\text{Ratio} = \frac{\text{Measurement Signal}}{\text{External Reference Signal}}$$

More details are supplied in Section 3.4.12.

3.5.29.2 The Measurement and Reference signals are connected to the DMM's signal and reference input terminals. Table 3.14 indicates how the GPIB Signal/Reference Commands V0 and V1 determine which Input terminals are used for Measurement Signal and Reference Signal connection. Note that the External Reference input terminals cannot be used for ohms measurements.

3.5.29.4 When in Software Ratio mode, the time to complete a reading can be calculated from Figure 3.25 or Figure 3.26, which, along with the GPIB throughput calculations in paragraph 3.7, supply the necessary information to calculate the time required to program, trigger, and transfer a reading back to the controller.

3.5.29.5 EXTERNAL REFERENCE FUNCTION COMMANDS.

3.5.29.5.1 External reference function commands are used to select the voltage reference used by the digital multimeter in making measurements. The controller may select the normal internal reference (ratio disabled) or an external ratio reference. Transmission of the G0 program code by the controller causes the DMM to use internal reference for all measurements. When using the instrument in the external reference mode, the reference is applied to the Signal or External Reference inputs as shown in Table 3.14.

3.5.29.5.2 When using a DC external reference, the user first connects the signal and reference as described above and then transmits the program code G1. For AC external reference, the same hook up is made followed by a G2 command. For ohms external reference, either the G3 or G4 commands may be used.

3.5.29.6 EXTERNAL REFERENCE RANGE COMMANDS

3.5.29.6.1 There are six ranges for external reference signals applied to the Input connector of the DMM. These are listed in Table 3.12 under the Operation column heading. When using an external reference in remote mode, the controller must transmit the appropriate program code Q3 through Q8 to select the correct range. Q0 selects the reference auto-range function.

3.6 TIME-OUTS: A PRACTICAL TREATISE.

3.6.1 TIME-OUTS are variable delays which are inserted at the proper point in the measurement sequence in order to guarantee that the signal has settled sufficiently before a reading is taken.

3.6.2 Like many other Racal-Dana DMM's, these Models provide 2 types of time-outs. Together, these time-outs reduce the burden on the GPIB programmer because most of the system timing problems involving insufficient

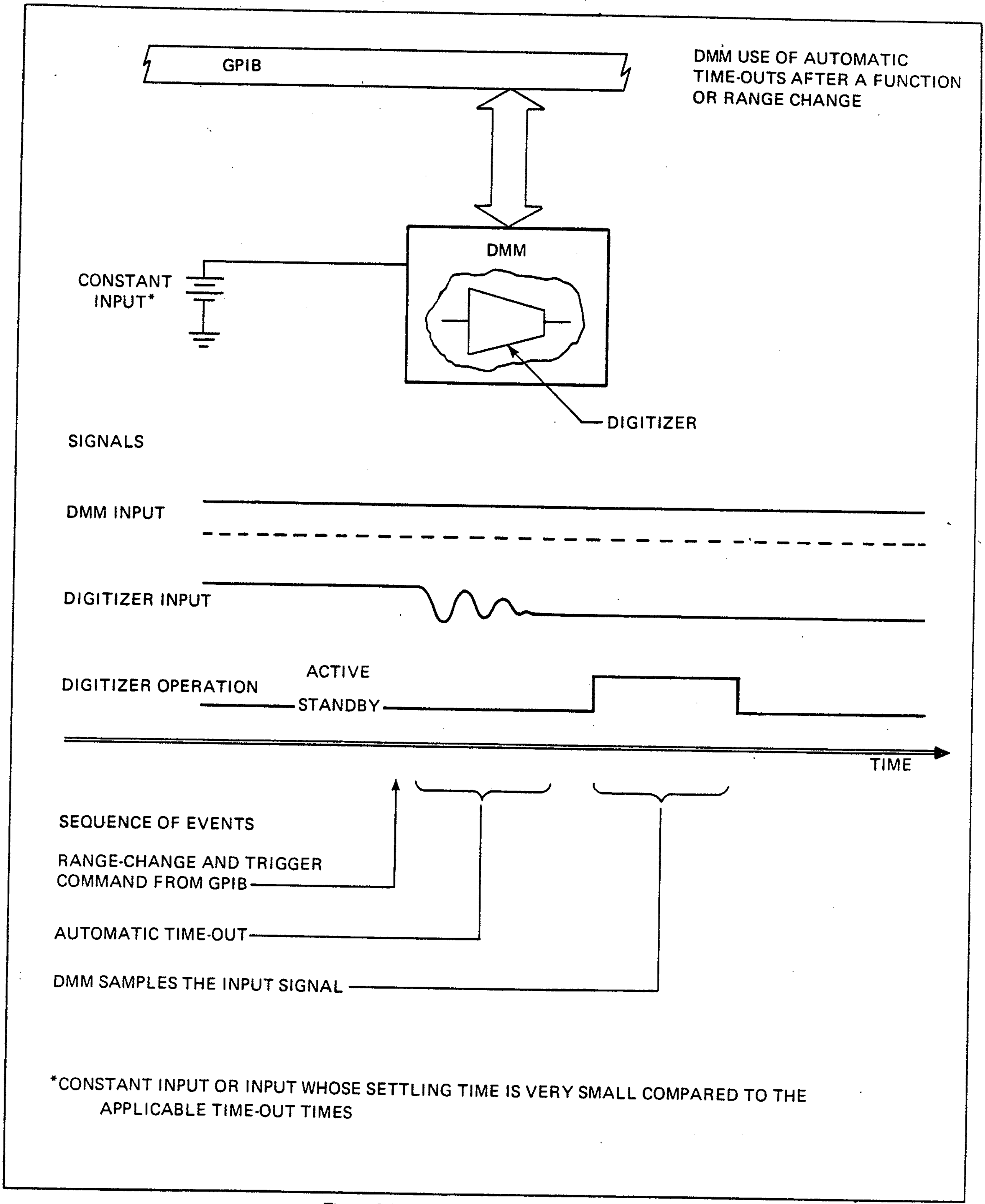


Figure 3.23 - DMM Automatic Time-Out

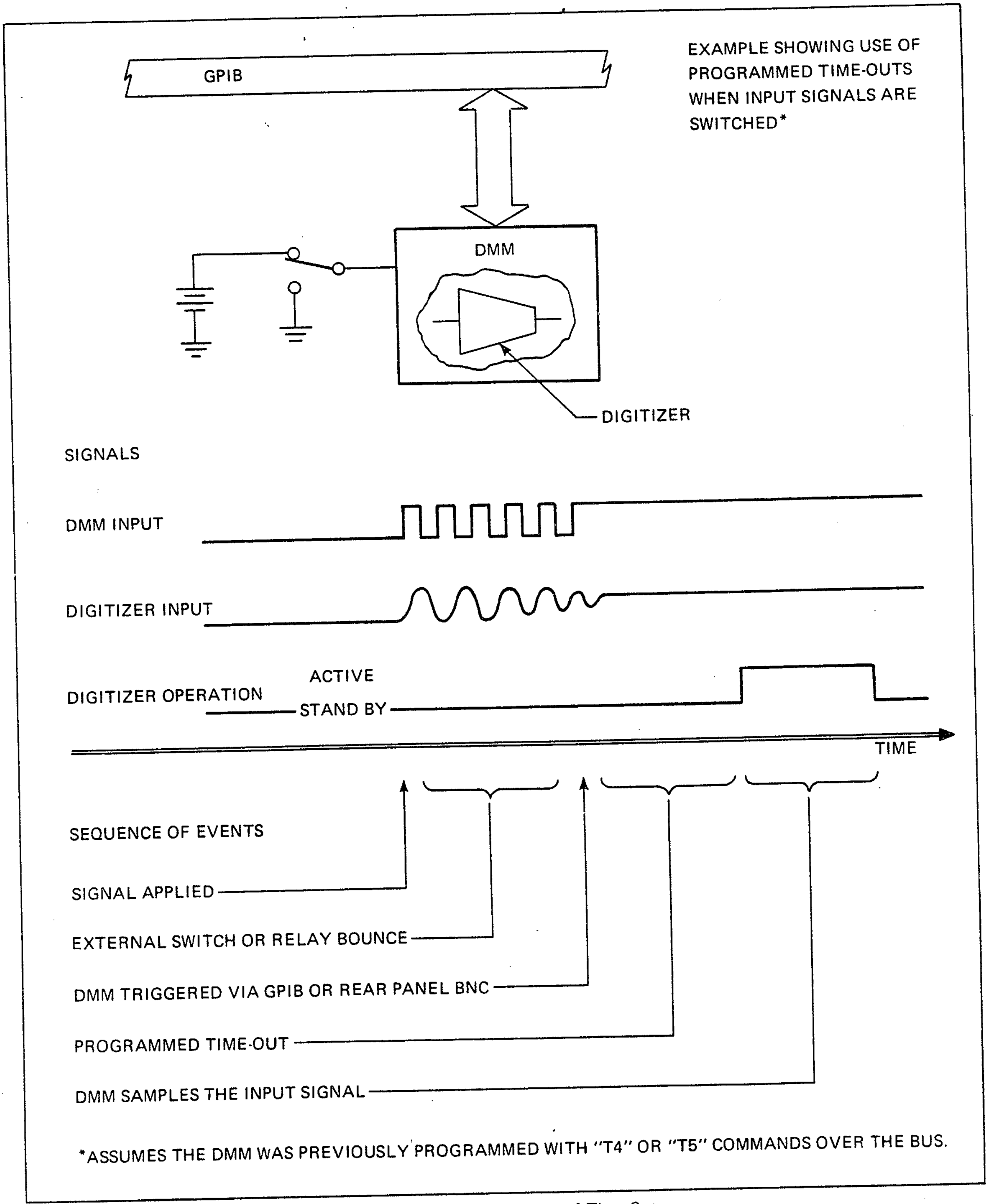


Figure 3.24 - DMM Programmed Time-Out

settling times and first reading errors are taken care of automatically inside the DMM. "First Reading Error" is an erroneous reading output by an instrument immediately following a function or range change.

Table 3.15 - Time-Out Times

Function	Time-Outs	Digits Error	
		5 1/2 Mode	4 1/2 Mode
DC	30 mS	10	1
AC*	400 mS	100	10
KΩ .1-1K	40 mS	10	1
10K	300 mS	10	1
Any Function Plus Filter	500 mS	10	1

*Time-out will be insufficient if incoming signal has a DC level other than zero volts.

3.6.3 Table 3.15 lists the time-out times and also lists the remaining digits of error which are not compensated for by the time-outs.

3.6.4 When any DMM is being programmed and triggered over the GPIB, a typical chain of events may occur something like this:

1) Apply input signal to DMM.
2) Program DMM and trigger reading.
3) Take reading from DMM.

Figure 3.23 shows this sequence graphically and also shows how the DMM automatic timeout feature prevents it from outputting bad data after a function, range change, or other GPIB command. Notice in the figure that the input signal is assumed to have already settled before the sequence begins.

3.6.5 Another chain of events which commonly occurs is listed below. This situation is found more often when many inputs of the same type are being measured:

1) Apply input signal to DMM.
2) Trigger DMM (without changing function or range).
3) Take reading from DMM.

Figure 3.24 shows this sequence and also shows how the use of programmed time-outs (T4 and T5 commands) allow the programmer to pass the responsibility for settling time over to the DMM. Here again it is assumed that the input signal has already settled before the DMM is triggered, since it would be impossible for the DMM to compensate for an unknown settling time caused by conditions external to the DMM.

3.6.6 In the previous paragraphs it was mentioned how the DMM handled its own settling time problems in various ways, but no mention was made of how the programmer might deal with settling time problems which originate external to the DMM. When low impedance measurements are being made, the main cause of delay times external to the DMM occur either in the signal source or in the signal scanner. Unless compensated for, these delays can cause large measurement errors.

3.6.7 One way of dealing with this situation is to place a delay in the controller's software between the signal setup routines and the DMM trigger routines, thus guaranteeing that the signal has settled before the DMM is triggered. A complication arises because the required delay time may vary considerably depending upon which signal source function and range is selected, etc. In systems where test time is not critical, the programmer may decide to use the worst case required delay during all measurements.

3.6.8 If throughput is a consideration, the programmer may decide to use a variable delay which depends upon the selected signal source and scanner settings, but this approach may require intimate knowledge of the devices' internal workings or repeated experimentation. Recently another alternative has been made available in the form of smart signal sources and scanners which can control system timing to guarantee that the signal has settled before the next operation is allowed to proceed. One example of this class of smart scanners is the Racal-Dana Model 1200. When programmed to do so, it will hold off further GPIB activity until all of its relays have switched to their new positions and have ceased bouncing. In most cases this guarantees that the Model 1200's output signal has completely settled before the controller has a chance to trigger the measurement device.

3.7 GPIB THROUGHPUT CALCULATIONS: A PRACTICAL TREATISE.

3.7.1 This section which presents GPIB Throughput Calculations is included as an aid to systems designers who must determine how much time is required to program, trigger, and obtain a reading from the DMM when operated over the GPIB.

3.7.2 The HANDSHAKE TIMES listed in Table 3.16 are typical times required to handshake characters over the bus. These numbers can be used to estimate the bus time required

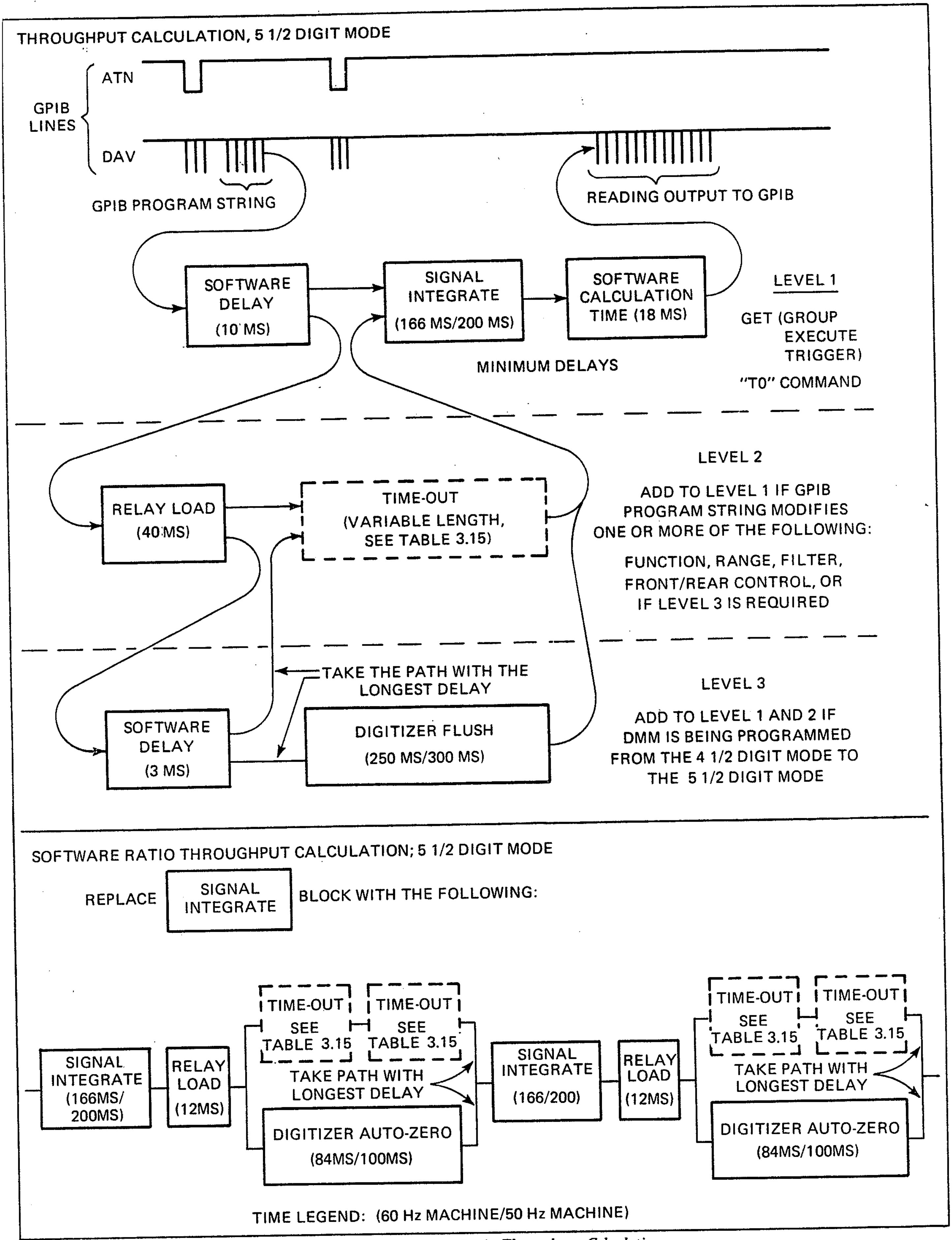


Figure 3.25 - 5 1/2 Digit Software Ratio Throughput Calculation

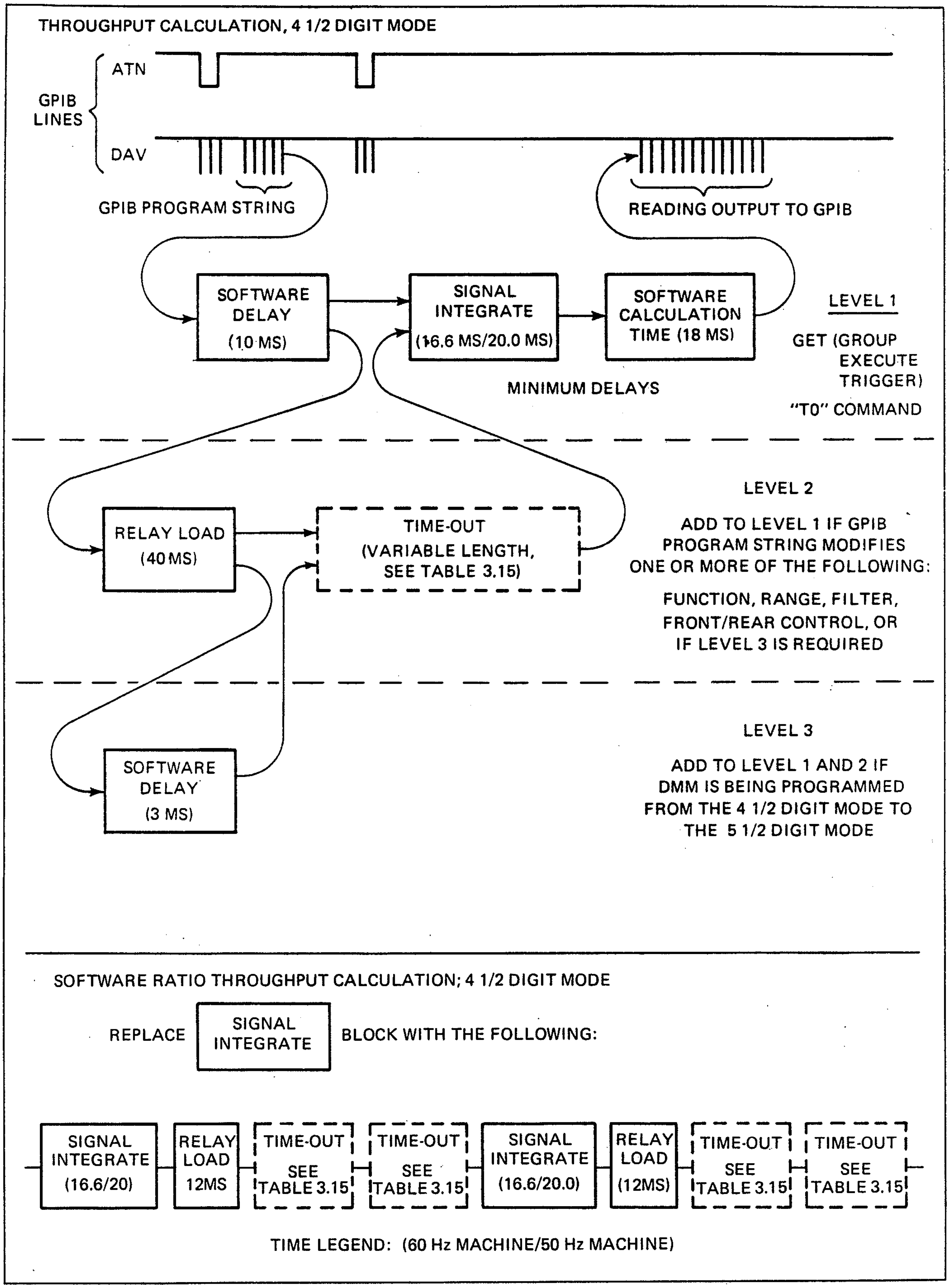


Figure 3.26 - 4 1/2 Digit Software Ratio Throughput Calculation

to exchange various data. For an example, to transmit the string "F1R5CRLF" to the DMM (6 characters) 400 μS/character = 2.4 mS are required approximately.

3.7.3 The time necessary to PROGRAM, TRIGGER and OUTPUT a reading from the DMM is presented in Figure 3.25 and Figure 3.26. The Figure 3.25 is used when in the 5 1/2 digit mode or when in the 4 1/2 digit mode and the DMM is being programmed to the 5 1/2 digit mode. Figure 3.24 is used when the DMM is in the 4 1/2 digit mode or when the DMM is being programmed from 5 1/2 to 4 1/2 digit mode. Notice that the times shown do not include the actual bus time necessary to transfer data to or from the DMM, but this time can be estimated using Table 3.16. The throughput equations shown in the preceding 2 figures are based upon the assumption that the DMM is in 'HOLD' and is waiting to be triggered or re-programmed. This assumption is made because when not in hold, delays become much more difficult to estimate due to the random timing between incoming GPIB commands and readings already in progress. Since this section is an aid to computing the time required to obtain a reading, it is also assumed that each program string contains a DMM trigger such as the "T0" command, or is followed closely by a GET (Group Execute Trigger). This accounts for the 2 figures showing a Signal Integrate delay and also showing a reading being output to the GPIB.

3.7.4 Both Figures 3.25 and 3.26 show 2 GPIB lines at the top of the page. These are shown for reference only, and to identify when bytes are being transferred to or from the DMM. To ease the task of calculating DMM throughput, each figure is divided into three levels. Level 1 delays are the minimum delay that can occur whenever the DMM is programmed over the bus. GPIB commands which cause only level 1 delays are those commands which cause no modifications to the configuration. Examples of these are trigger commands, Null commands, R0 (auto-range) command, and Z (initialize) command. These are all processed very rapidly, and the majority of level 1 delays occur due to the "T0" or GET (Group Execute Trigger) which is assumed to accompany the program string.

Table 3.16 - Typical GPIB Handshake Times

Bus Operation	Typical Time Req.
Handshake Interface Messages	12 μS
Handshake and Process an Incoming String of Characters	400 μS/Character
Output the Serial Poll Status Byte	300 μS
Output a Reading (15 Characters)	130 μS/Character

3.7.5 If the GPIB command modifies one or more of the following: function, range, filter, front/rear control, then level 2 delays should be added to level 1 delays when performing delay calculations. Examples of commands which will cause a level 2 delay are: F1 (DC) if the DMM is in some other function, or R5 (10V range) if the DMM is in some other range. Note that level 2 delays will only occur if the GPIB command modifies the function, range, etc. For instance, if the DMM is already in DC and the "F1" command is sent, only level 1 delays will occur. Level 3 delays should be added if the DMM is being programmed from one digit mode (integrate time) to another. For example, if the DMM is in the 4 1/2 digit mode and an "I2" or "I3" command is received, the DMM will experience level 3 as well as level 1 and 2 delays.

3A.1 Purpose.

3.A.1.1. The section contains Manual and System application examples for the digital multimeter. Each example contains a statement of purpose along with keyboard or GPIB programming details. Paragraph 3A.2 presents the Manual application while paragraph 3A.3 presents the GPIB system application using an HP 9825 calculator connected to the DMM through the IEEE-488-1978 Standard Interface.

3A.2 Manual Applications.

3A.2.1 Purpose: Configure the DMM and 1200 Scanner to do the following:

a) Scan 5 noisy input signals at 1 hour intervals.

b) Read each input signal 4 times and average the 4 readings to reduce noise effects.

c) Store the averaged readings to the DMM's Data Buffer for later recall.

3A.2.2 The DMM's Time function will be used to sequence the measurements, and the LAH function will be employed to average 4 readings into one to reduce noise effects. The 1200 scanner will accept trigger pulses from the DMM which will cause it to scan to the next channel. To prepare the Model 1200, do the following:

a) Turn AC power off.

b) Remove all relay cards except one, which should be installed in the location nearest to the power switch.

c) When triggered, the Model 1200 will scan channels 1, 2, 3 ... 9, 10 and then back to 1, etc. Since only 5 signals are to be scanned, the 10 channels should be paralleled as shown in Figure 3A.1 (see 1200 manual for hookup details peculiar to the switch decade assembly being used).

3A.2.3 After connecting the 1200 and the DMM as shown in Figure 3A.2 and applying power, the key sequence shown in Table 3A.1 is performed. The DMM will then begin sequence described below.

a) The system will remain dormant for approximately 12 minutes.

b) The DMM will take 4 readings at one-second intervals and average them.

c) The averaged reading will then be copied into the Data Buffer and also displayed.

d) The DMM will send a pulse to the scanner, causing it to sequence to the next input. (Go to step a)).

3A.2.4 The timing diagram in Figure 3.29 shows the system timing as the first two inputs are measured, averaged, and stored into the buffer memory. Notice that as the sequence begins, no relay channels are selected. This causes the contents of buffer location 0 to be unuseable. Valid data can be found starting with buffer location 1.

3A.2.5 The need for noise rejection required that the Time Function's subinterval and N registers be used to trigger multiple readings for averaging purposes. If this requirement did not exist, these Time registers could instead be used to allow the sampling of all 5 inputs within seconds of one another. The following changes would be required to bring this about:

a) LAH function disabled.

b) 1.0 programmed as Time 3 (Interval = 1 hour).

c) .0001* programmed as Time 4 (Subinterval = 1 second).

*2-4 seconds may be required for certain combinations such as Filter + Autorange.

d) 5 programmed as Time 5 (Number of readings = 5).

e) The Model 1200 should be pre-triggered, causing the first channel to be selected.

The resulting timing diagram is shown in Figure 3A.4.

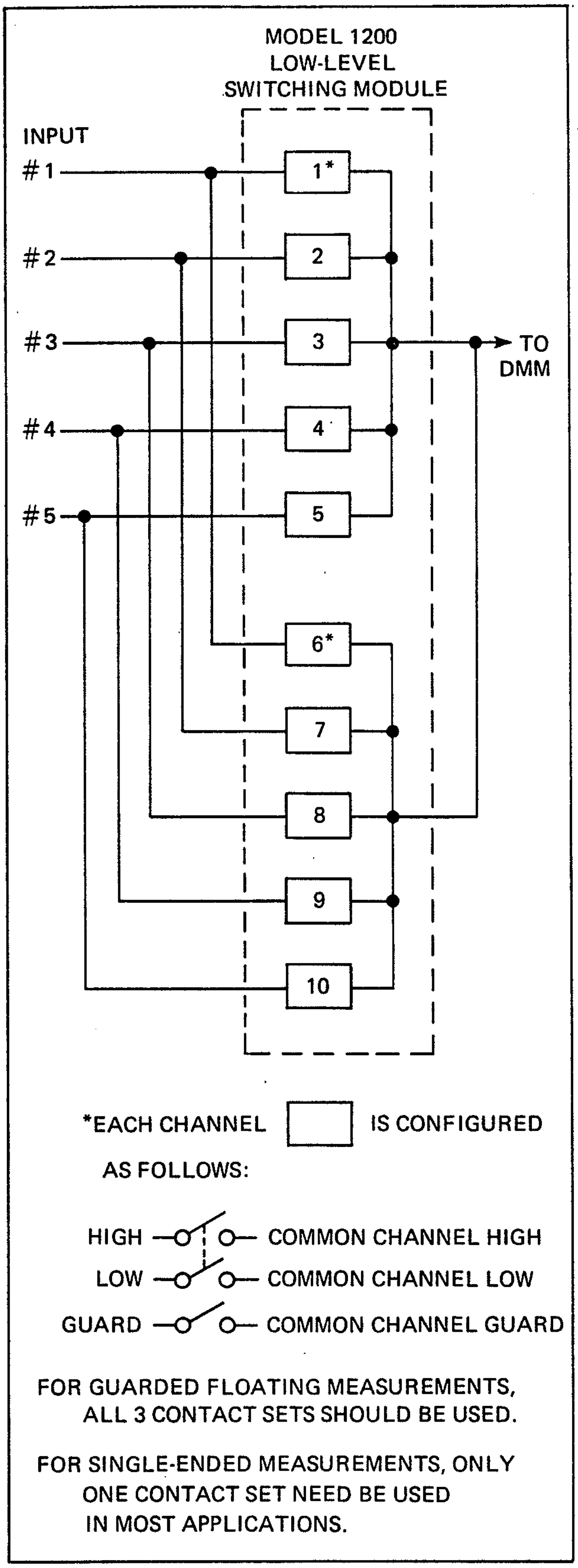


Figure 3A.1 - Wiring of Switching Module For Bench Application # 1

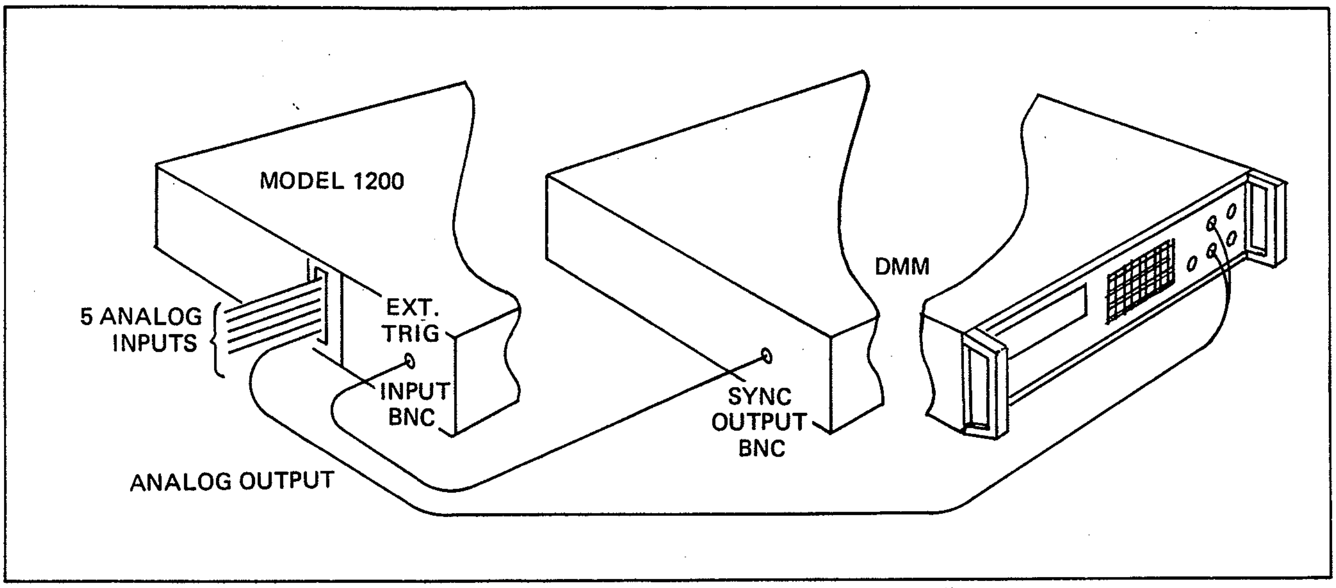


Figure 3A.2 - Signal Connections For Bench Application # 1

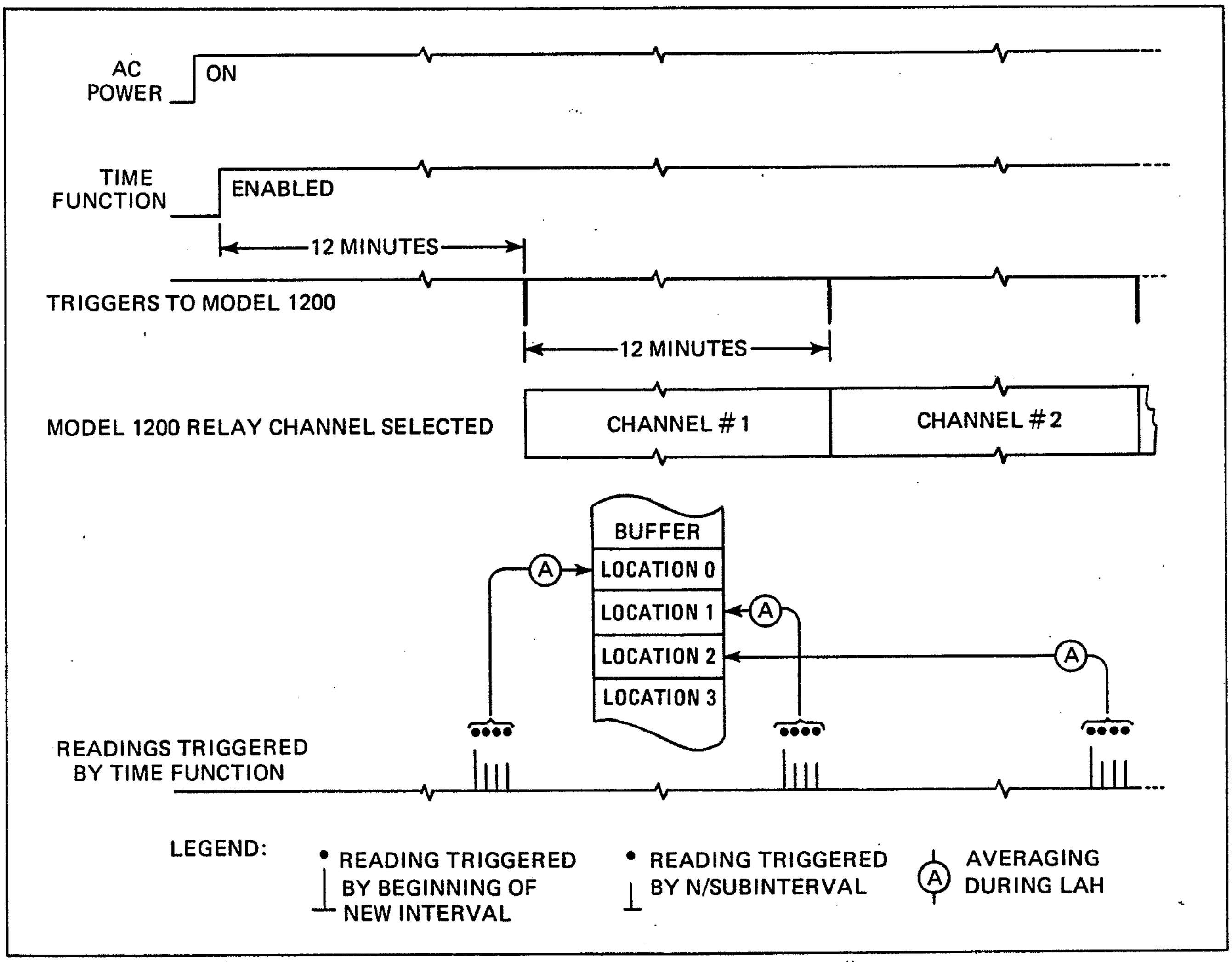


Figure 3A.3 - Read Timing For Bench Application # 1

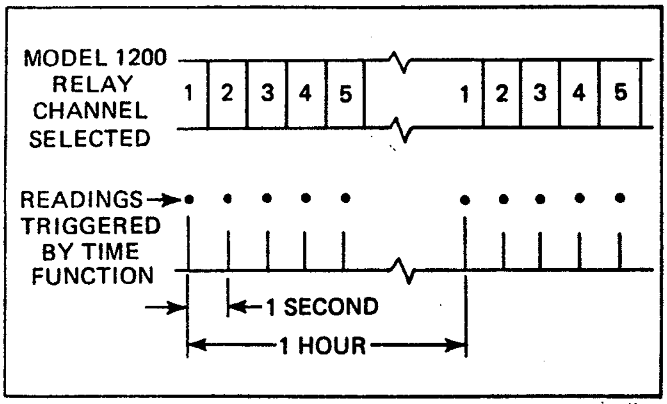


Figure 3A.4 - Modified Read Timing For Bench Application #1

3A.3 System Applications.

3A.3.1 Each System Application example contains a program listing as printed by a calculator along with an explanation for each line of the program. If the DMM is to be used with a Hewlett-Packard Model 9825 calculator the programming presented in this section may be used directly and/or further modified to suit the users needs. Because the DMM may be used with any controller which operates on the standard interface bus the user may wish to prepare equivalent software for another controller device. In such a case the user should review the remote operating instructions contained in Section 3 of this manual to select and assemble appropriate operating statements for his controller which cause the transmission of the required interface messages and device dependent messages.

3A.3.2 For example, in the first program sample in this section, line zero of the program is `rem 7` and the accompanying explanation indicates that this statement on the Hewlett Packard 9825 calculator sends the remote message to all devices on the bus. This statement causes the calculator to lower the REN line thus arming the DMM for remote operation.

3A.3.3 Referring again to the first example note that line 1 of the program printout contains the statement `flt 6` and that the accompanying explanation indicates that this sets the floating decimal format. This may or may not be a feature or function of the controller in use and since it is not an interface or device dependent message use of an equivalent is at the discretion of the user. Line 2 of the program shows the statement `wrt 702, "zF1r5"`. The explanation indicates that this transmits the device listen address 02. The user should select the statement for his controller which causes it to transmit the listen address assigned to the DMM. Instructions for the address assignment of the DMM are presented in paragraph 3.5.5. Table 3.8 shows the address switch setting, the talk and listen address characters and data line binary code for each available decimal address of the instrument.

Table 3A.1 - Key Sequence For Bench Application #1

Step	Key Sequence	Comments
1.	SHIFT	Press the SHIFT key as required. Note SHIFT annunciator for correct execution.
2.	RESET	Clear all ESC functions.
3.	SHIFT 0 STORE TIME 1	Set start time to 0.
4.	SHIFT 9 9 STORE TIME 2	Set stop time to infinity.
5.	SHIFT ● 1 2 STORE TIME 3	Set interval to 12 minutes (= 1 hour/5).
6.	SHIFT ● 0 0 0 1 STORE TIME 4	Set subinterval to 1 second.
7.	SHIFT 4 STORE TIME 5	Set N to 4 readings.
8.	SHIFT 4 STORE LAH	Set LAH Average Cycle constant to 4.
9.	SINGLE	Place instrument in Hold mode.
10.	BUFF	Clear Data Buffer by depressing Buff key until word "CLRBUF" appears on display
11.	LAH	Enable LAH and select Average by depressing LAH key until "A" appears, then release key.
12.	TIME	Enable Time function.

3A.3.4 Line 2 of the example also contains the program string which is composed of the device dependent messages. The device dependent message is the primary subject to which this section of the manual addresses itself. The examples contained in this section are presented primarily to show the various combinations of device dependent messages used to accomplish the various remotely controlled measurement operations. Note that the program printout indicates the string of device dependent messages presented in the table directly above the program tape. This format is maintained throughout the section and thus the user may use this section conveniently by referring to the device dependent message string shown for each system operation example.

3A.3.5 Line 3 of the program shown in the example instructs the DMM to become a talker and transmit the measurement data. Line 3 also instructs the calculator to store the measurement data transmitted by the DMM in a storage register known as "Variable A" and subsequentially to print the value in Variable A on the program tape. The final line on the program printout is the measurement value `7.985702e 00` the answer 7.9857 volts.

3A.3.6 The accompanying pages present eight remote systems applications, listed sequentially one through eight. Tables and figures are included throughout the examples to assist in following the explanations.

System Application # 1

Purpose: Remotely program the DC volts function to measure 7.9857 volts.

Program String: ZF1R5

Device Dependent Messages

Device Code	Parameter
Z F1 R5	Initialize, Internal Trigger DC Volts Range 5 (10 volts)

Program tape	
`0: rem 7`	Sends Remote Enable message to all devices on the bus.
`1: flt 6`	Sets floating decimal (scientific notation) format. Six places to the right of the decimal point, i.e., X.XXXXXXeXX.
`2: wrt 702,"zF1r 5"`	Address device 02 (DMM) as listener and writes device dependent message followed by a Carriage Return (CR) and Line Feed (LF) to device 02 (DMM).
`3: red 702,A`	Address device 02 (DMM) as a talker. Reads value into variable A from device 02 (DMM).
`4: prt A`	Prints the value stored in variable A.
`*9597`	
`7.985702e 00`	Answer: 7.9857 volts.

System Application # 2

Purpose: Remotely program the DMM to zero itself against an externally-supplied short circuit, and to perform limited self-tests.

Program String: F1R3K2

Device Code	Comments
F1	DC volts
R3	Range 3 (0.1 volts)
K2	Zero command

Program	Comment
`0: rem 7`	Sends Remote Enable message to all devices on the bus.
`1: wrt 718,"c1"`	Addresses device 18 (RD1200) as listener and writes a device-dependent message which causes the Model 1200 to switch a short circuit across the DMM's input terminals.
`2: wrt 702,"f1r3k2"`	Addresses device 02 (DMM) as listener and writes a device-dependent message followed by a Carriage Return (CR) and Line Feed (LF) to device 02 (DMM).

System Application # 3

Purpose: Remotely program the DMM to the "Hold" mode and trigger 3 readings, each time using a different technique to trigger and/or recover the reading.

Program String: ZT3F1R5T0
D1T0
D1

Program Code	Explanation
Z	Initialize
T3	"Hold" mode
F1	DC
R5	Range 5 = 10V range
T0	Trigger 1 reading
D1	SRQ when data is ready

(No. 3 continued)

Program	Description
`0: rem 7`	Sends Remote Enable message to all devices.
`1: wrt 702,"zt3f1r5t0"`	Address device 02 (DMM) as listener and writes device-dependent message followed by a Carriage Return (CR) and Line Feed (LF) to device 02 (DMM).
`2: red 702,A`	Address device 02 as a talker. Reads value into Variable A from device 02 (DMM).
`3: wrt 702,"d1t0"`	Address device 02 (DMM) as listener and writes device-dependent message followed by a Carriage Return (CR) and Line Feed (LF) to device 02 (DMM).
`4: oni 7,"GETUM"`	Upon receiving a Service Request (SRQ) from the bus, the controller will interrupt its present task and transfer control to the line labeled "GETUM" (line 16).
`5: eir 7`	Enable interrupts from the bus.
`6: gsb "OTHERTASK"`	Go to subroutine "OTHERTASK" while waiting for the reading to complete.
`7: wrt 702,"d1"`	Address device 02 (DMM) as listener and writes device-dependent message followed by a Carriage Return (CR) and Line Feed (LF) to device 02 (DMM).
`8: trg 702`	Address device 02 (DMM) as listener and send Group Execute Trigger.
`9: eir 7,0`	Disable interrupts from the bus.
`10: gsb "OTHERTASK"`	Go to subroutine "OTHERTASK" while waiting for the reading to complete.
`11: if band(rds(702),1)=0;gto 10`	Reads the DMM's status byte and checks to see if the Data Ready bit is set. If not, repeat subroutine "other task".
`12: red 702,C`	Address device 02 as a talker. Reads value into Variable A from device 02 (DMM).
`13: fxd 6;prt A,B,C`	Sets the format for printer output and prints variables A, B and C.
`14: stp`	Stops program execution.
`15:`	
`16: "GETUM":if band(rds(702),1)=0;eir 7;iret`	Interrupt Routine: Reads the DMM's status byte and checks to see if the Data Ready bit is set. If not, enable the interrupt once again and return from interrupt.
`17: red 702,B`	Address device 02 as a talker. Reads value into Variable A from device 02 (DMM).
`18: iret`	Return from interrupt.
`19:`	
`20: "OTHERTASK":` `21: wait 1000` `22: ret` `*26549`	Subroutine "Othertask" executes while controller is waiting for DMM's reading to complete. A simple delay is used in this example, but useful work can take place while waiting for readings.
`0.240918` `14.993000` `14.569900`	Printout of Variables A, B and C.

System Application #4

Purpose: Remotely program the Ohms function and compensate for (2-wire) lead resistance by storing a reference reading as the Null constant and enabling the Null function.

Program String: ZF3R3
N2N1

Device-Dependent Messages:

Device Code	Parameter
Z	Initialize, Internal trigger
F3	Ohms function
R3	0.1K Ohm range
N2	Store as Null constant
N1	Enable Null function

```
0: rem 7
1: wrt 702,"zf3R
 3"
2: red 702,A
3: wrt 702,"n2n1
 "
*19432
```

- 0: Sends Remote Enable message to all devices on the bus.
- 1: Addresses device 02 (DMM) as listener and writes a device-dependent message followed by a Carriage Return (CR) and Line Feed (LF) to device 02 (DMM).
- 2: Address device 02 (DMM) as a talker. Reads value into Variable A from device 02 (DMM). This program line ensures that a reading is completed before the next program line is executed.
- 3: Addresses device 02 (DMM) as listener and writes a device-dependent message followed by a Carriage Return (CR) and Line Feed (LF) to device 02 (DMM).

System Application #5

Purpose: Remotely program the DMM to trigger itself at high speed and store the resulting readings to the Data Buffer. The first 120 readings are then retrieved from the Data Buffer over the bus.

Program String: ZI1R5CO
C1

Device Code	Comments
Z	Initialize, Internal Trigger
I1	High-Speed Mode (4-1/2 Digits)
R5	Disable Autorange
CO	Clear the Data Buffer
C1	Output Data Buffer to GPIB

Program	Description
`0: dim A[120]`	Dimension an array of numerical variables A[1] through A[120].
`1: rem 7`	Sends Remote Enable message to all devices on the bus.
`2: wrt 702,"zi1r5c0"`	Addresses device 02 (DMM) as listener and writes a device-dependent message followed by a Carriage Return (CR) and Line Feed (LF) to device 02 (DMM).
`3: wait 5000`	Wait 5 seconds (can be 4 seconds if DMM has 60 Hz option).
`4: wrt 702,"c1"`	Addresses device 02 (DMM) as listener and writes a device-dependent message followed by a Carriage Return (CR) and Line Feed (LF) to device 02 (DMM).
`5: for N=1 to 120`	Beginning of For-Next loop. This line, along with the following 2 lines sequence the transfer of 120 readings from the DMM's data buffer to the array A[1] through A[120].
`6: red 702,A[N]`	Addresses device 02 (DMM) as a talker. Reads value into variable A[N] from device 02 (DMM).
`7: next N`	Last line of For-Next Loop.
`*8739`	

System Application # 6

Purpose: Remotely program the LAH function to average readings in groups of 5, and then output the average to the display and to the bus.

Program String: Z 5L6L3

Device Code	Comments
Z	Initialize, Internal Trigger
L6	Store Entered Constant (5.0) as the LAH Average cycle count, C .
L3	Enable LAH and select the Average as the Output.

Printout	Comments
`0: rem 7`	Sends Remote Enable message to all devices on the bus.
`1: wrt 702,"z5L6 L3"`	Addresses device 02 (DMM) as listener and writes a device-dependent message followed by a Carriage Return (CR) and Line Feed (LF) to device 02 (DMM).
`2: red 702,A`	Addresses device 02 (DMM) as a talker. Reads value into variable A from device 02 (DMM).
`3: fxd 6;prt A`	Sets the format for printer outputs and prints variable A (see below).
`4: gto 2` `*29822`	Causes program to loop from line 2 through line 4.
`-0.000041`	Average of readings 1 to 5.
`-0.000041`	Average of readings 6 to 10.
`-0.000041`	Average of readings 11 to 15.
`-0.000043`	

System Application #7

Purpose: Remotely program the DMM to capture the minimum and maximum percentage deviation over a series of 10 or more readings*.

Program String: Z R5 3.75P2P1 10LGL3
L7

Device Code	Comments
Z	Initialize, Internal Trigger
R5	Range 5 (10V or 10KΩ range)
P2	Store entered constant (3.75) as the percent constant
P1	Enable Percent function
L6	Store entered constant (10.0) as the LAH cycle count C
L3	Enable LAH and select the Average as the output
L7	Transmit LAH constants: Low, Average, High, N, C

*A slow controller may have difficulty retrieving the LAH constants before an 11th reading has been completed. In this case the LAH constants will be affected by 11 readings rather than 10.

If desired, the controller can use the D1 command to cause a single SRQ to be issued after the tenth reading, thus allowing the controller's response to be interrupt-driven rather than polling the DMM as shown below.

Program line	Description
`0: rem 7`	Sends Remote Enable message to all devices on the bus.
`1: wrt 702,"zr5 3.75p2p1 10L6L3 "`	Addresses device 02 (DMM) as listener and writes a device-dependent message followed by a Carriage Return (CR) and Line Feed (LF) to device 02 (DMM).
`2: red 702,A`	Addresses device 02 (DMM) as a talker. Reads value into Variable A from device 02 (DMM). This program line ensures that 10 readings have been completed before the next program line is executed.
`3: wrt 702,"L7"`	Addresses device 02 (DMM) as listener and writes a device-dependent message followed by a Carriage Return (CR) and Line Feed (LF) to device 02 (DMM).
`4: red 702,L,A,H`	Addresses device 02 (DMM) as a talker. Reads value into variables L, A and H from device 02 (DMM). Note that the L7 command made 5 numbers available for output but only the first and third are of interest in this application, therefore the 4th and 5th are not read.
`5: fxd 6;prt L,H` `*13982`	Sets the format for printer output and prints variables L and H (see below).
`-10.124700`	Lowest Percentage deviation from 3.75.
`-6.364260`	Highest Percentage deviation from 3.75.

System Application # 8

Purpose: Remotely program the Software Ratio and Null functions along with the Interrupt commands to do the following:

a) Configure the DMM as an AC ratiometer with a 1-10 VAC signal applied to the rear input and a 30 VAC reference connected to the front input terminals.

b) Use null along with the Interrupt commands so that the controller receives an SRQ if the ratio reading is less than 0.36.

Program String: ZF2R5V1G2Q0 .36N2N1D2

Device Code	Comments
Z	Initialize, Internal Trigger
F2	AC Volts
R5	Range 5 (10V range)
V1	Rear Input
G2	External Reference, AC function
Q0	External Reference Autorange
N2	Store entered constant (0.36) as Null constant
N1	Enable Null function
D2	Send SRQ if reading –Null is negative

```
0: rem 7
```
Sends Remote Enable message to all devices on the bus.

```
1: wrt 702,"zf2r
.5v1g2q0 .36n2n1
d2"
```
Addresses device 02 (DMM) as listener and writes a device-dependent message followed by a Carriage Return (CR) and a Line Feed (LF).

```
2: if band(rds(7
02),1)=0;jmp 0
*18721
```
Checks bit DIO1 of the serial poll status byte from device 02 (DMM). If bit DIO1 is zero (Data not ready), the line is executed again.

Execution continues on next line (not shown) if bit DIO1 of the DMM's status byte is set. This will occur only if a ratio of less than 0.36 is measured by the DMM.

4.1 GENERAL.

4.1.1 This section presents the circuit description for the DMM as the signal propagates from the input terminals to the front panel display or the rear panel General Purpose Interface connector. The text will refer to simplified diagrams, schematics and other aids which may be required to enhance the general description.

4.1.2 The physical configuration drawing illustrated in Figure 4.1 is an exploded chassis view which displays the DMM main sections comprising the main PCB. The numbers identified with each section are the discussion sequence followed in the text. The DMM block diagram is presented on Figure 4.1A.

4.2 POWER SUPPLIES.

4.2.1 The DMM is designed to operate from a wide range of AC line voltages and frequencies with 120 VAC and 60 Hz considered standard. The transformer design includes a selectable multi-tapped primary winding to accommodate line voltages of 100, 120, 220, and 240 VAC ± 10%, 47 through 440 Hz. A multi-tapped secondary with three separate windings develop the low voltage DC supplies required to power the DMM circuits.

4.2.2 The primary windings are wrapped with a shield, transformer terminal 6 and the shield is connected to the DMM chassis. The chassis is connected to power line ground through the power receptacle, J209. The analog windings have two additional shields for maximum isolation and common mode rejection. The guard shield, transformer terminal 18 extends through the analog section of the PCB with two aluminum shields guarding the analog circuits. The inner shield, transformer terminal 17 is connected to analog common.

4.2.3 From the three secondary windings, low voltage DC supplies are generated to power the main sections of the DMM. The voltage levels designators and grounds appearing

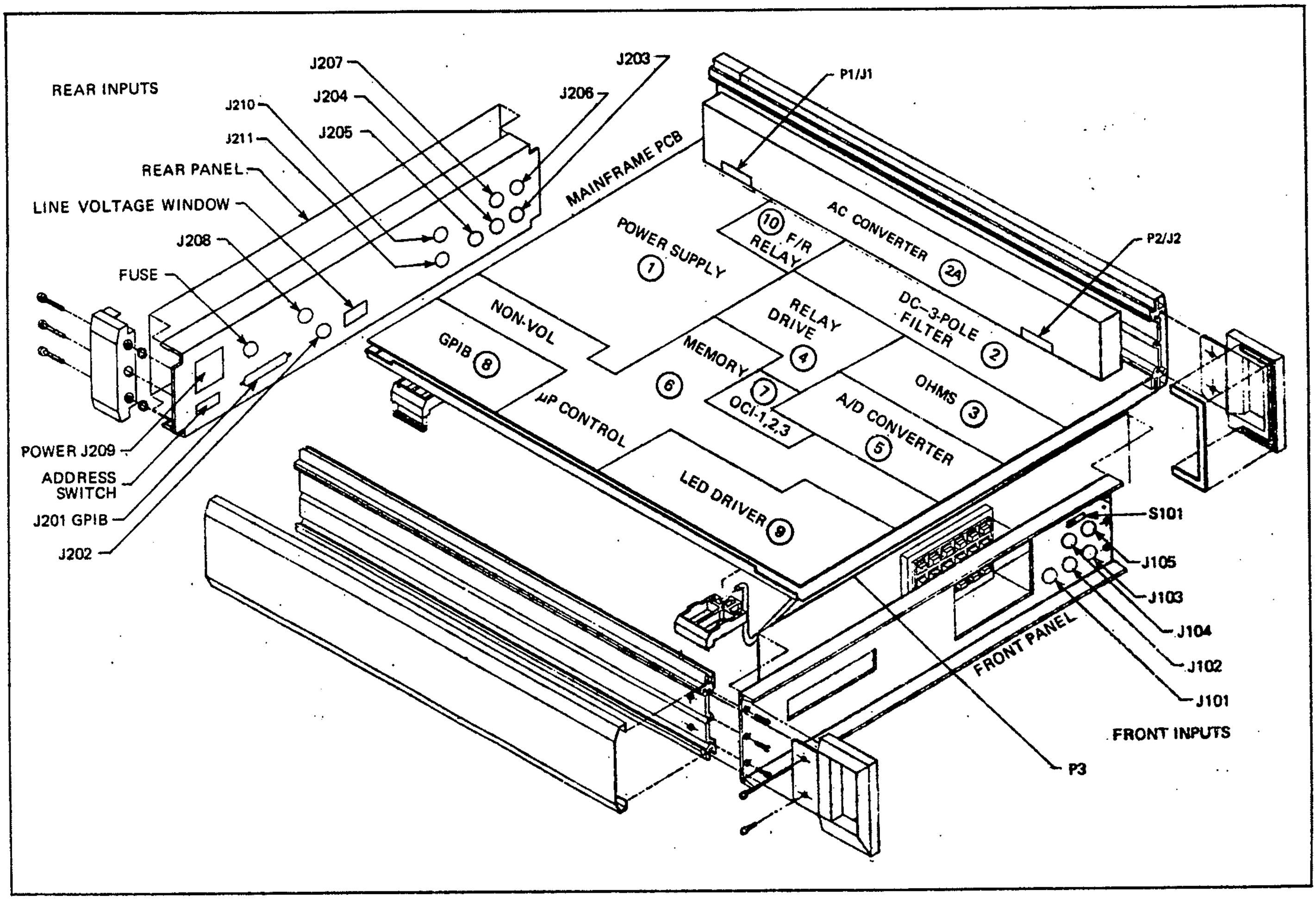


Figure 4.1 - DMM Sectional Drawing

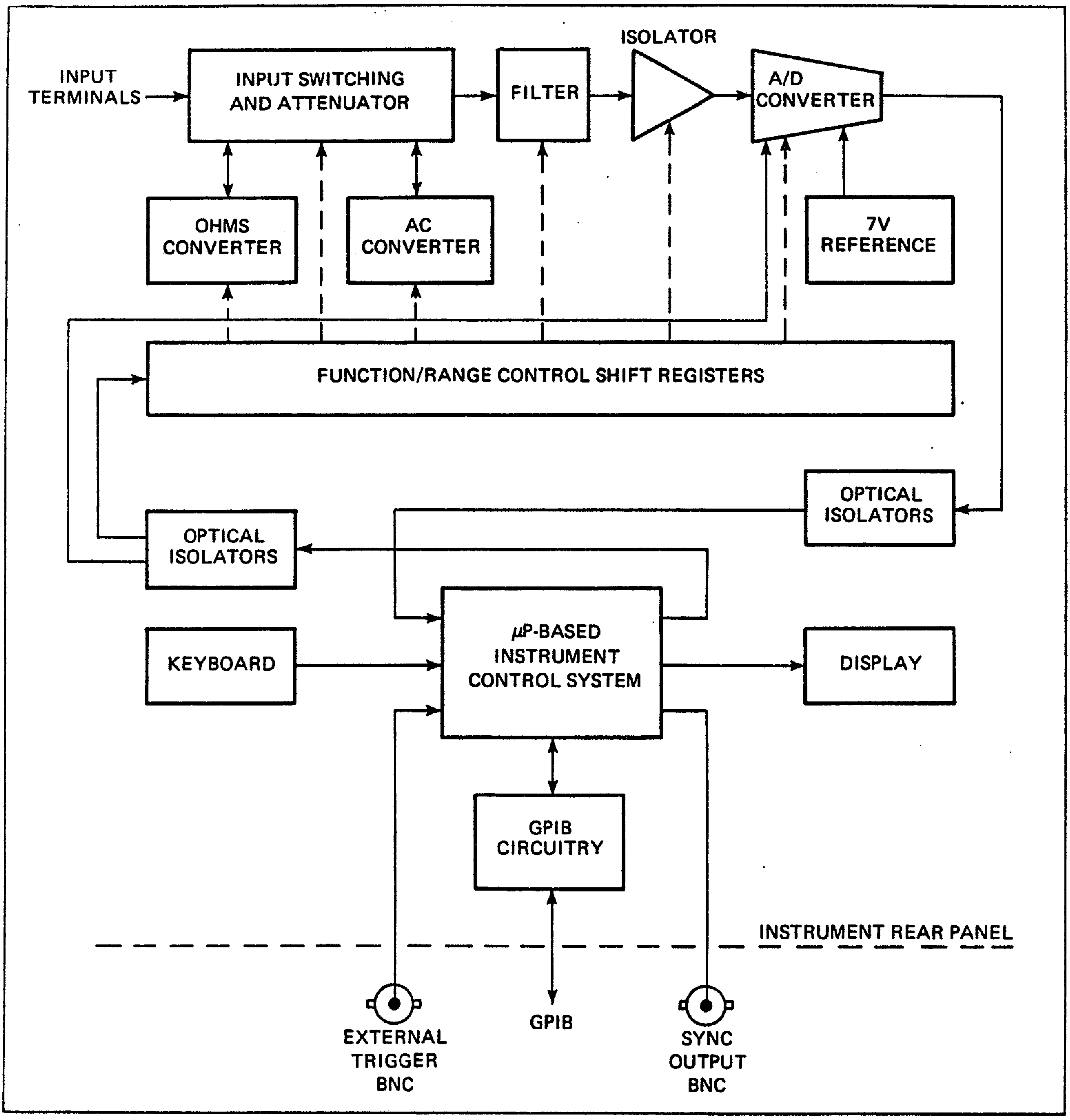


Figure 4.1A - DMM Block Diagram

on the power supply schematic, page 6-5, are used on all schematics; this is a sound troubleshooting aid.

4.3 ANALOG SUBSECTION.

4.3.1 Analog Hardware.

4.3.1.1 The Analog section of the DMM is positioned in the Guard area of the PCB assembly. This includes Section 2, 3, 4 and 5 of the board as shown in Figure 4.1, an exploded view of the DMM.

4.3.1.2 The Analog section, as shown in block diagram Figure 4.2, consists of the following basic subsections: Input Attenuator, Selectable 3-pole Active Filter, Variable gain Isolator, Variable gain AC Scaling Amplifier, True RMS or average AC converter, Ohms Amplifier and a Variable Ohms Current Source. A description for each function follows in this section.

4.3.2 Function and Range Switching.

4.3.2.1 The DMM's Function and Range are controlled by keyboard inputs, or GPIB commands. Upon receiving these signals, the microprocessor sends a new bit pattern to the function/range control shift-registers in order to energize the proper relays, and supply proper logic levels to other hardware.

4.3.2.2 The relays controlling the Function selection are K1, K8, K11 and K12. The relay closures for each function are tabulated in the following chart.

Table 4.1 - Function Relay Chart

FUNCTION	K1	K8	K11	K12
DC				
AC				■
OHMS	■	■	■	■

■ ENERGIZED

In the DC Function, all Function relays are de-energized and DC measurement signals are routed through the DC Input attenuator to the Isolator. In the AC Function, K12 is energized routing the input signal to the AC converter. The output signal from the AC converter is applied to the DC Input attenuator. Attenuator relay K9 is energized in AC and OHMS ranges and does not attenuate the AC converter output as the signal inputs the Isolator.

4.3.2.3 In the OHMS Function, relays K1, K8 and K11 are energized, switching the Ohms Current Source and Ohms Amplifier into the configuration shown in Figure 4.4. The Function relay chart, Table 4.1 indicates the energized relays for the Ohms Function. The ranges for DC and ohms are selected by relays K2, K3, K4, K5, K6, K7 and K9. The Range Relay chart for DC and ohms is shown in table 4.2, the next chart.

Table 4.2 - Range Relay Chart

FUNCTION	RANGE	K2	K3	K4	K5	K6	K7	K9
DC	.1V							■
	1V							■
	10V							■
	100V							
	1KV							
OHMS	.1KΩ					■	■	■
	1KΩ					■		■
	10KΩ	■		■				■
	100KΩ		■	■				■
	1000KΩ			■				■
	10,000KΩ				■			■

■ ENERGIZED

This group of relays direct and scale the signal from the INPUT terminals to the Isolator input. The Isolator output signal voltage is scaled by Q15, 16, 17 and K9 as listed in Table 4.3, the Isolator Range chart.

4.3.3 DC Volt Function.

4.3.3.1 The DMM is basically a DC measuring instrument. The DC signal conditioner, which is common to AC and OHMS, performs three functions: scaling the input signal to

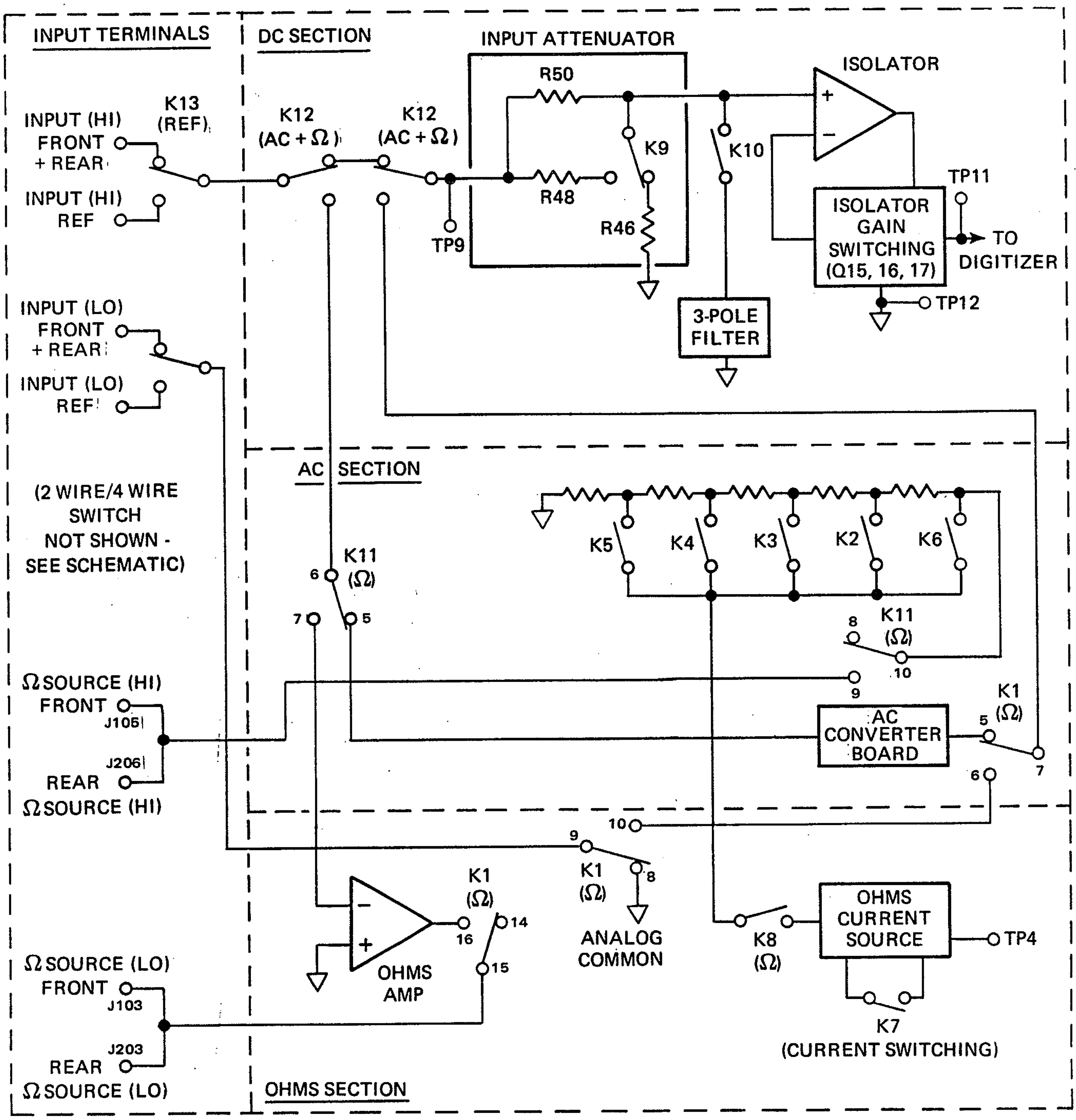


Figure 4.2 - Analog Signal Conditioning Block Diagram

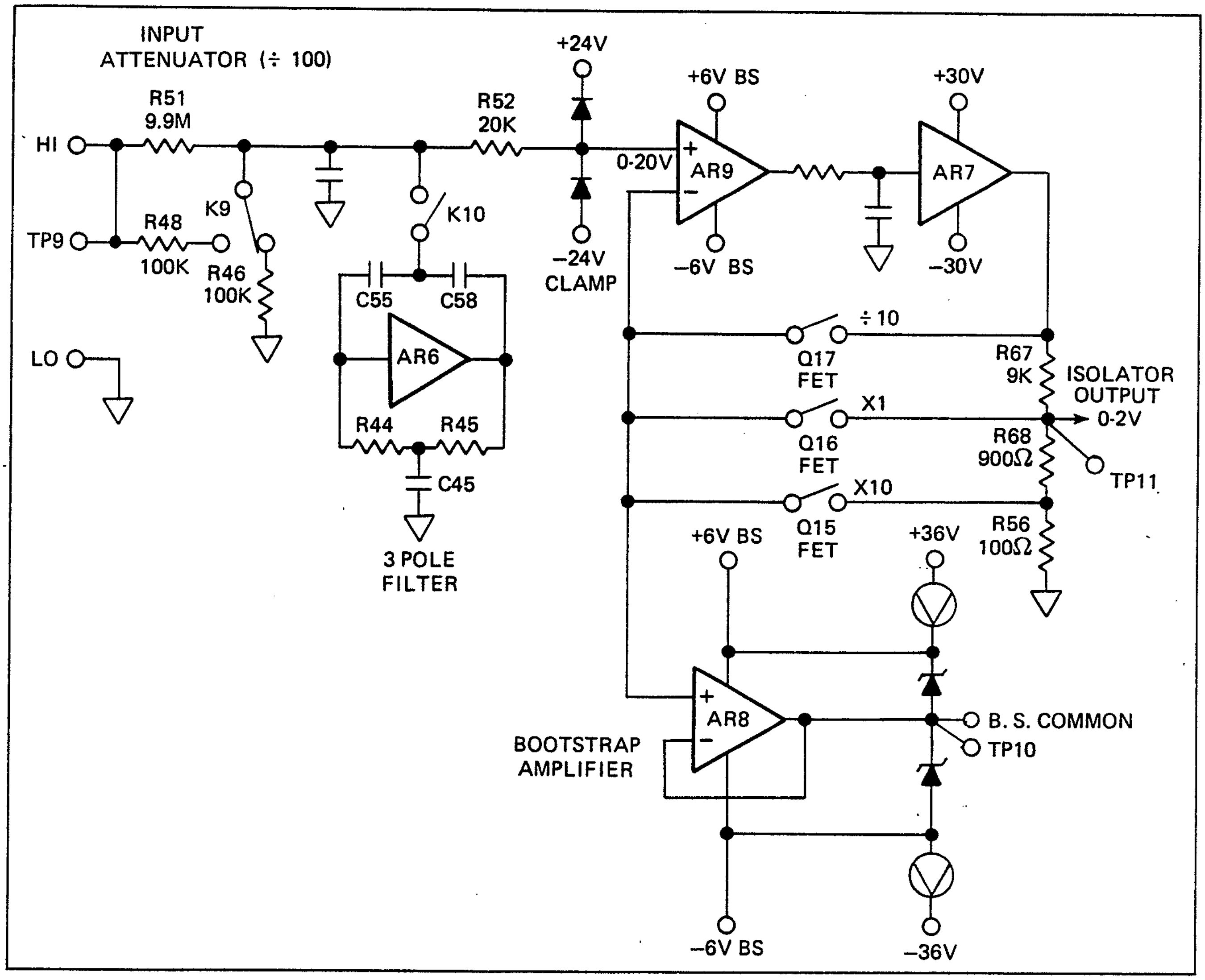


Figure 4.3 - Isolator and Bootstrap Amplifier

one volt full scale; filtering the signal to reduce unwanted noise; isolating the source from loading effects. The DC signal conditioning is performed by the Input Attenuator, Isolator, and Filter. A simplified diagram of this circuit is shown in Figure 4.3. The complete block diagram showing the relationship to other parts of the analog section is shown in Figure 4.2.

4.3.3.2 The DC signal applied to the DMM INPUT terminals is routed through the reference relay K13 and AC relay K12 to the DC input attenuator. If the .1,1 and 10 volt range is selected, the Attenuator relay K9 is energized and the input voltage is routed with no attenuation to the Isolator input. In this mode R48 parallels R51. This provides overload current limiting and forms part of the three-pole active filter. If the 100 or 1K volt ranges are selected, K9 is de-energized, completing a voltage divider of R51 and R46, attenuating the input signal 100:1 before application to the Isolator.

4.3.3.3 A User selectable three-pole active filter is switched in or out of the circuit at the Isolator input by relay K10. The filter consists of op-amp AR6, capacitors C45, C55, C58 and resistors R44, R45. Relay K10 can be enabled either via the keyboard or GPIB. The filter provides attenuation of noise frequencies above 10 Hz. Filter response is at least 35 dB down at 50 Hz and attenuates 18 dB/Octave to –60 dB or greater.

4.3.4 Isolator.

4.3.4.1 The Isolator contains an Input-Clamp, a high open-loop gain amplifier, bootstrap amplifier, and a gain switching network controlled by the range and function logic. A simplified diagram is presented in Figure 4.3 and the Isolator Range chart is shown in Table 4.3.

Table 4.3 - Isolator Range Chart

RANGE	K9	Q16	Q15	Q17	ISOLATOR GAIN
	÷ 100	X1	X10	÷ 10	
.1V	■		■		10
1V	■	■			1
10V	■			■	.1
100V		■			1
1000V				■	.1

■ RELAY ENERGIZED OR FET SWITCH ON.

4.3.4.2 The Isolator accepts varying voltages at its input from zero to ± 20 VDC, depending on the signal input and the range selected. The amplifier is non-inverting with a closed loop gain of 10, 1 or 0.1 depending on the DMM range selected. Inputs are thus scaled to ± 1 volt full scale level (± 2 volts with 100% over-range) and applied to the Digitizer. Input overloads are clamped at ± 24 volts.

4.3.4.3 The non-inverting configuration combined with the bootstrap amplifier increases the input resistance of the Isolator to over 1000 megohms. A high open loop gain is achieved by the use of two operational amplifiers, AR9 and AR7. The output of AR7 is applied to a feedback network consisting of R67, R68 and R56. Listed next is Table 4.4, which charts scale factors for the Isolator gain-switching (or attenuation) and Figure 4.3 shows a simplified diagram of the Isolator feedback network.

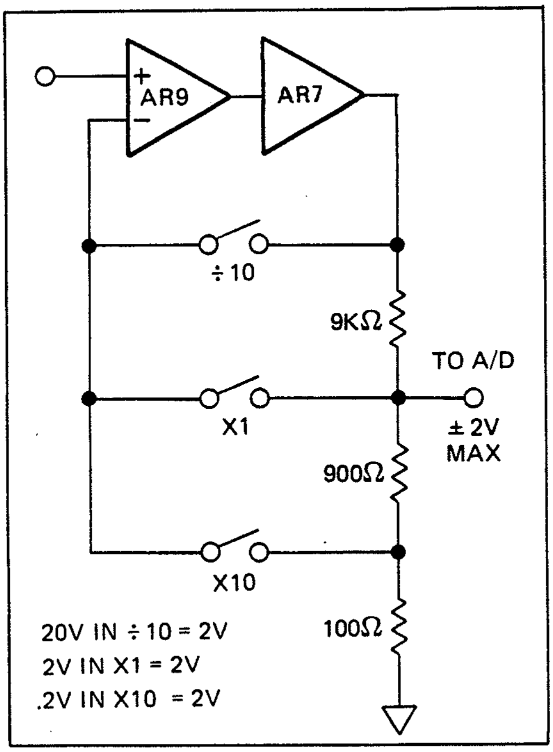
When FET switch Q17 is closed, the output of AR7 is connected directly to the inverting input of AR9 as negative feedback. The closed loop gain to the output of AR7 is ONE, but since the output is tapped from the junction of R67 and R68, the overall Isolator gain is 0.1. When Q17 is closed, the overall gain is ONE and closing Q15 provides a gain of 10.

4.3.4.4 The BOOTSTRAP amplifier, AR8 and associated components, senses the Isolator feedback voltage (which tracks the input) and provides bootstrapped voltages (BSV) approximately 6 volts higher and 6 volts lower than the input to power AR9. The ± BSV on AR9 tracks the input to the Isolator which increases its input resistance above the level achievable without BSV. The output from AR7 (BS COMMON) drives the input bias current network to prevent it from shunting the input resistance.

4.3.5 Ohms Function.

4.3.5.1 The resistance measurement system shown in Figures 4.4 and 4.5 contain the ohms amplifier, voltage reference, current source, open input clamp and input over-voltage clamp. In operation, a fixed and stable current source is generated for each range and the current is fed through the resistance to be measured. The voltage drop across the resistor is proportional to the unknown resistance Rx. This voltage is read by the DMM and displayed as kilohms on the display. The current supplied provides a full scale DMM reading when the unknown resistance is equal to the range selected. For an example, the measuring of 10 kilohms on the 10 K range produces a DMM readout of 10.0000.

Table 4.4 - Isolator Gain Switching



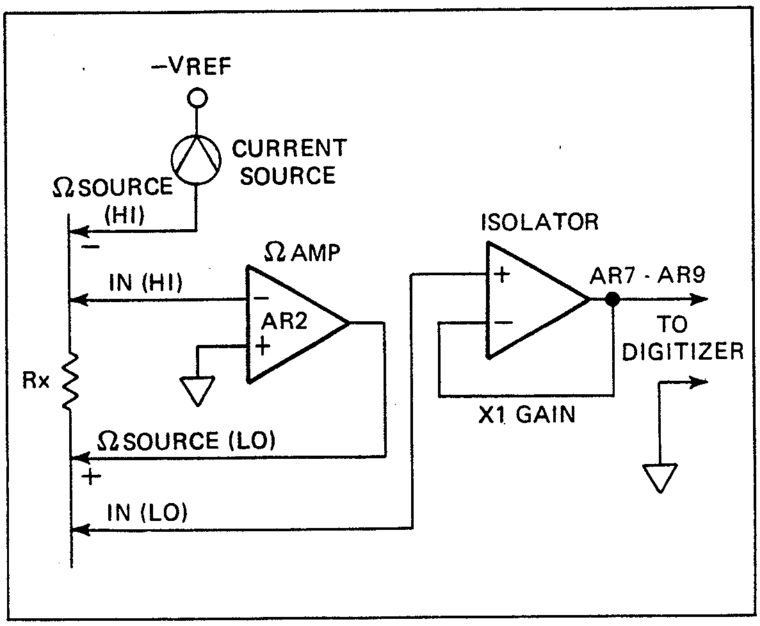


Figure 4.4 - Resistance Measurement System

4.3.5.2 The Ohms current source utilizes an accurate reference voltage to generate a reference current source through the resistor divider and current switching network, refer to Figure 4.5. An open input-clamp is also part of the ohms converter circuit. The ohms voltage reference is a 7 volt temperature-stabilized zener, VR2. The 7 volt reference is buffered by the ohms current source generator op-amp AR1. The current through darlington transistor pair Q7 and Q8 is determined by R31 and R35. This network supplies 1 mA or 10 mA to the current-divider network. Relay K7 switches R35 in parallel with R31 to generate the 10 mA current source. The lower Ω source currents required for the 10K, 100K, 1000K and 10,000KΩ ranges are established by dividing the Ohms CURRENT SOURCE output. The current divider consists of R25, R27, R28, R29 and R33 and the division is controlled by range relays K2-K6. The ohms ranges, current sources and the range relays are shown in Table 4.4.

4.3.5.3 \The Open-Input clamp protects the user's external input from voltage increases when the ohms terminals are not provided with a resistive load, or during range overload. The input open circuit voltage is clamped at −6 volts maximum by Q3, Q5 and transistor array U3. U3 clamps the base of Q7 to −30 volts thereby turning off the current source through Q8 during overload. CR2, Q8 and VR3 protect the current source from voltages applied at the input terminals.

Table 4.5 - Ohms Range, Relay and I Source

RANGE	K2	K3	K4	K5	K6	K7	Ω SOURCE CURRENT
.1K					■	■	10 ma
1K					■		1 ma
10K	■		■				100 μa
100K		■	■				10 μa
1000K			■				1 μa
10000K				■			100 na

■ ENERGIZED

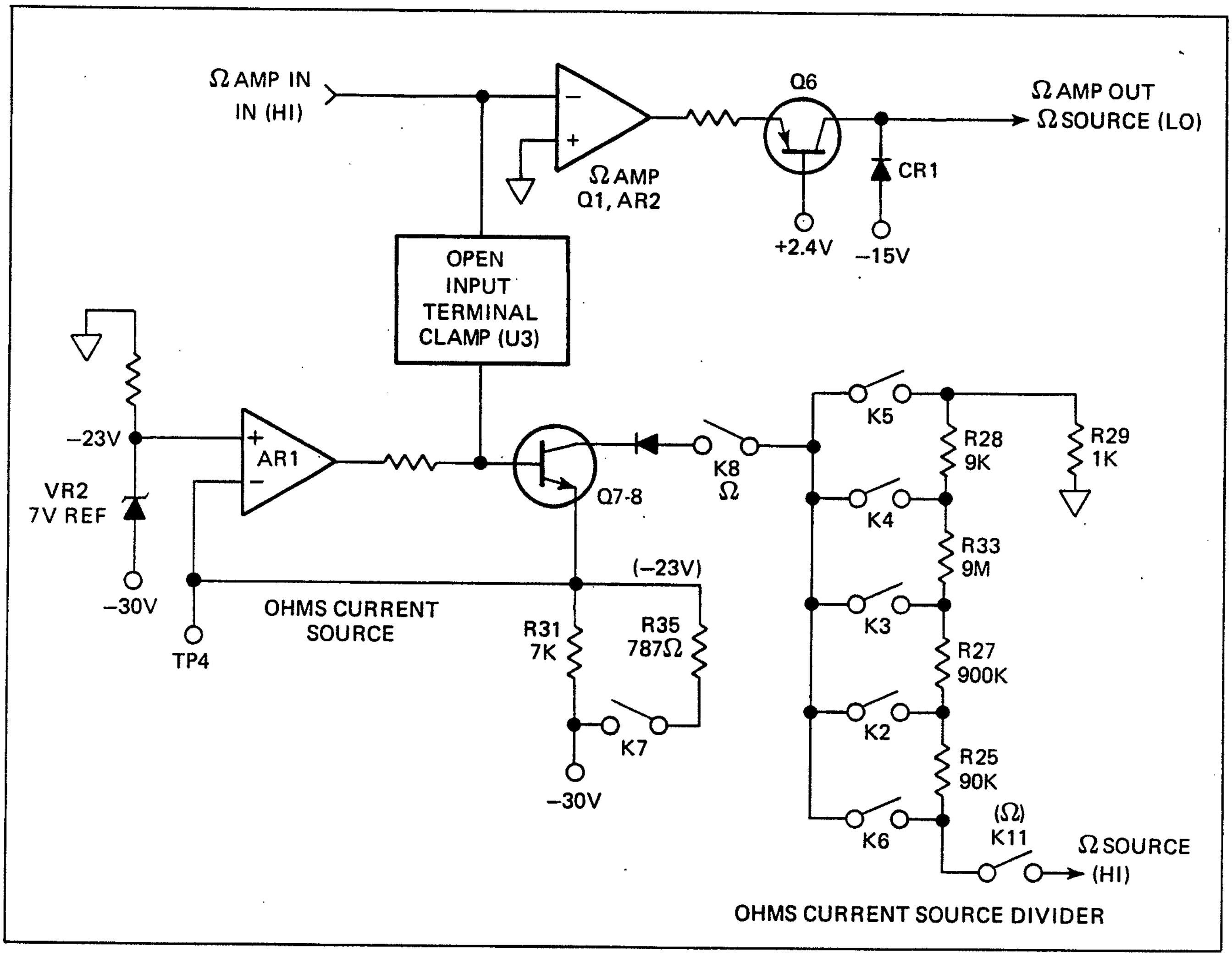
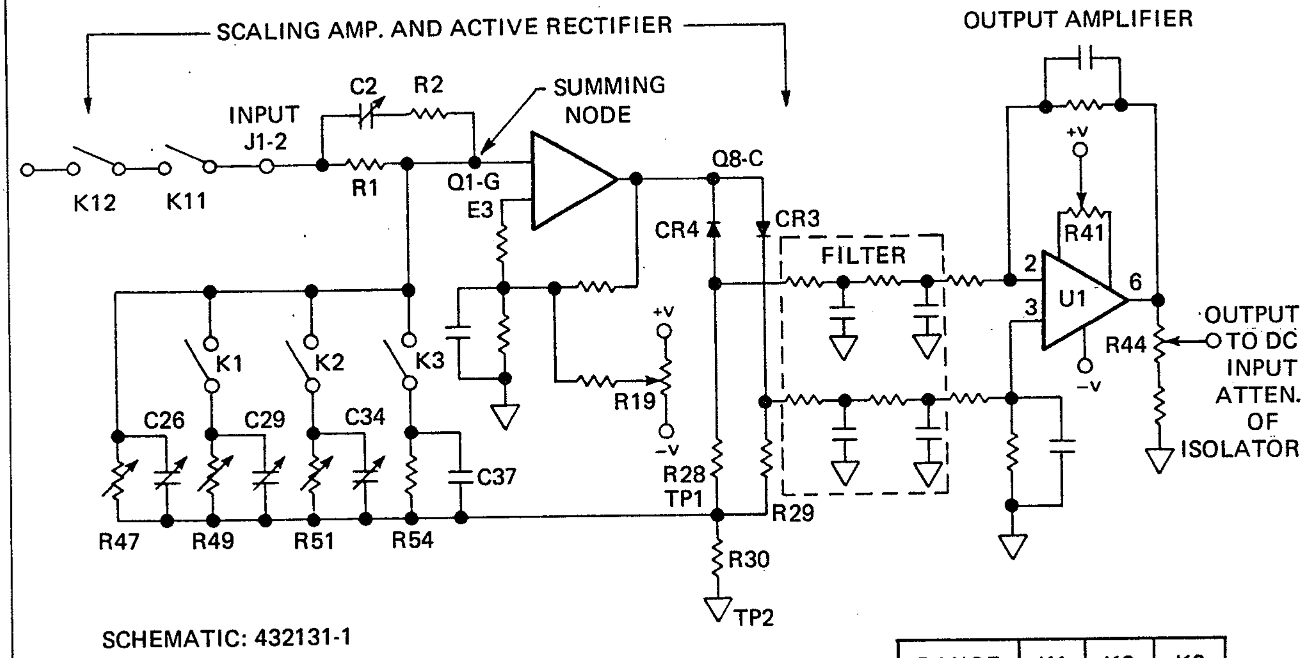


Figure 4.5 - Simplified Ohms Converter



RANGE	K1	K2	K3
1			
10	█		
100		█	
1000			█

█ RELAY CLOSED

Figure 4.6 - Averaging AC Converter

4.3.6 Averaging AC Converter (Model 5005)

4.3.6.1 The Model 5005 DMM features an averaging AC to DC converter that is assembled in a separate PCB located in section 2A of the DMM Sectional drawing Fig. 4.1, and plugs into connectors J1 and J2 on the motherboard. The AC converter is configured with a Scaling Amplifier Q1-Q8; Active Rectifier section CR3 and CR4; and a ripple filter network. The converter output amplifier employs U1 op-amp to generate –1VDC full scale.

4.3.6.2 From the inputs terminals, the AC input signal is switched to C1 coupling capacitor, through the AC relay K12 (energized) and through the ohms relay K11 (de-energized). The AC signal continues through the RC network of R1-R2-C2 to the input the summing node of the Scaling Amplifier. A simplified drawing of the AC assembly is shown in Fig. 4.6, a take-off from schematic drawing 432131-1.

4.3.6.3 The Scaling amplifier Input resistor R1, and selectable feedback resistors control gain of each range. Range relays K1-K3 select the feedback resistors for each range. The Scaling amplifier attenuates the input signal in the 1, 10, 100 and 1 KV ranges. Feedback on the 1V range is through the permanently connected resistor R46/47. The 10, 100, and 1 KV ranges have relay selected feedback that parallel the 2V network through R48&49, R50/51/52, and R53/54/55 respectfully. The output from the scaling amplifier is 1V for full scale in each range. The relay chart shown in Fig. 4.6, presents the relay states for each range selected.

4.3.6.4 The Scaling amplifier input is protected from overload voltages by diode clamp CR1 and CR2.

4.3.6.5 The active rectifier configuration has two distinct polarity feedback paths; the feedback path consisting of CR3 and R29 conducts current when the output of the amplifier is positive and the CR4 - R28 path conducts when the amplifier output is negative. The two currents are combined across resistor R30 and the resulting AC signal is fed through the range feedback network to the input summing node of the scaling amplifier. Two half-wave signals of opposite polarities are developed across resistors R28 and R29 for each full-wave input. These signals are filtered to a DC level and amplified by a gain of ten by the differential output amplifier U1 and routed to the DC input attenuator of the isolator. (−1V for full scale).

4.3.7 RMS AC Converter (Model 5006)

4.3.7.1 The Model 5006 DMM features an RMS AC to DC converter that is assembled on a separate PCB and located in section 1A of the DMM Section drawing Figure 4.1. The PCB plugs into connectors J1 and J2 on the motherboard. The RMS converter is configured with a Scaling Amplifier – Q3, AR1, range switching and input clamp networks; active DC Rectifier–Amplifier Q4 through Q9, CR1 and CR2; Logarthmic (log) Amplifier - Q10 through Q14; RMS Output Amplifier Circuitry - AR2, DC attenuator, and a ripple filter.

4.3.7.2 From the DMM input terminals, the AC signal is routed to C25 coupling capacitor, through the AC relay K12 (energized) and through the Ohms relay K11 (De-energized). The AC signal continues through the RC network of R57 and associated components to the input of the scaling amplifier. A simplified drawing of the RMS assembly is shown in Figure 4.7, a take-off from schematic drawing 432131.

4.3.7.3 The Scaling Amplifier (differential dual FET input, transistor Q3 and op-amp AR1) is an inverting operational amplifier that conditions the input signal and generates a full scale output of 1 volt AC in the 1V range. Signal attenuation for the 10, 100 and 1 KV ranges are developed by feedback resistors R7/8, R5/6 and R2/3 through range relays K3, K2 and K1 in the feedback circuit of AR1. The AC output signal from AR1 Pin 6 is routed via R19-5K and R24-20K resistor to the summing node of the log amplifier Q11 and to the input of Q5 the RMS converter circuitry. The Scaling Amplifier inputs (at Q3) is protected from overload voltages by transistors Q1, Q2, A15, and Q16 wired as diodes and connected as positive and negative voltage limiting clamps.

4.3.7.4 The Active Rectifier circuitry, which includes Q4 through Q9, CR1 and CR2, is configured as an op-amp with dual polarity feedback routes. One feedback route through CR1 and R21 conducts during the negative voltage excursions from the amplifier. During the positive voltage excursions, CR2 via R23 completes the feedback path to differential amplifier Q5. This half-wave positive-rectified signal also travels via R32-10K to the summing node of the log amplifier Q11; the input to the RMS converter circuitry.

4.3.7.5 The RMS converter (log amplifier Q11, Q12 and Q13; log feedback loop Q10A and Q14B) is configured as an operational amplifier with a logarithmic feedback loop. The output from the log amplifier (Q13 collector) is the log of the total summing node input to Q11 received via the Active rectifier, Scaling amplifier and the log exponential feedback voltage developed across Q14A and Q10A, and is proportional to the log of the rectified signal current.

4.3.7.6 The output from the log amplifier also drives the input network to AR2 op-amp that is identical to the log amplifier feedback loop which consists of Q14B and Q10B. This input network supplies current to the summing node of the output amplifier AR2 and converts the log amplifier output Q13 to an RMS current, with the AC component bypassed through C20. The DC component is fed through Q10B to the input of the output amplifier AR2. This current is converted to a 5 volt RMS voltage (for a full-scale input) at the output of the driver amplifier AR2. The RMS construction through the log amplifier can be itemized as noted next:

a) Q14B squares the signal - C20 averages it.
b) AR2 performs the averaging of the squared signal.
c) Q10B extracts the square root.

From the output driver amplifier, the 5 VRMS is filtered and attenuated in the output RC network to deliver a 1 volt full-scale level signal that is routed to the DC signal conditioner input.

4.3.7.7 Measurements may be made in the AC coupled mode (standard) or DC coupled mode (AC + DC). In the DC coupled mode S2 is switched, applying a short across C25 and S1 is switched, applying a short across C15. DC blocking capacitors C25 and C15 are active in the AC coupled mode only.

4.4 QUANTIZED FEEDBACK A/D CONVERTER.

4.4.1 General.

4.4.1.1 The A/D Converter uses a quantized feedback (QF) conversion technique to convert the analog output from the Isolator to a BCD format for further processing and display.

4.4.1.2 The A/D Converter hardware is located in Section 5 of the PCB assembly. The converter consists of A/D Analog Processor (U11), Digital Counter and Control I.C. (U10), Measure/Zero (M/Z) switch U26, Input Buffer AR5, Auto-Zero Buffer AR3, Auto-Zero switch Q9, Digit Mode switch

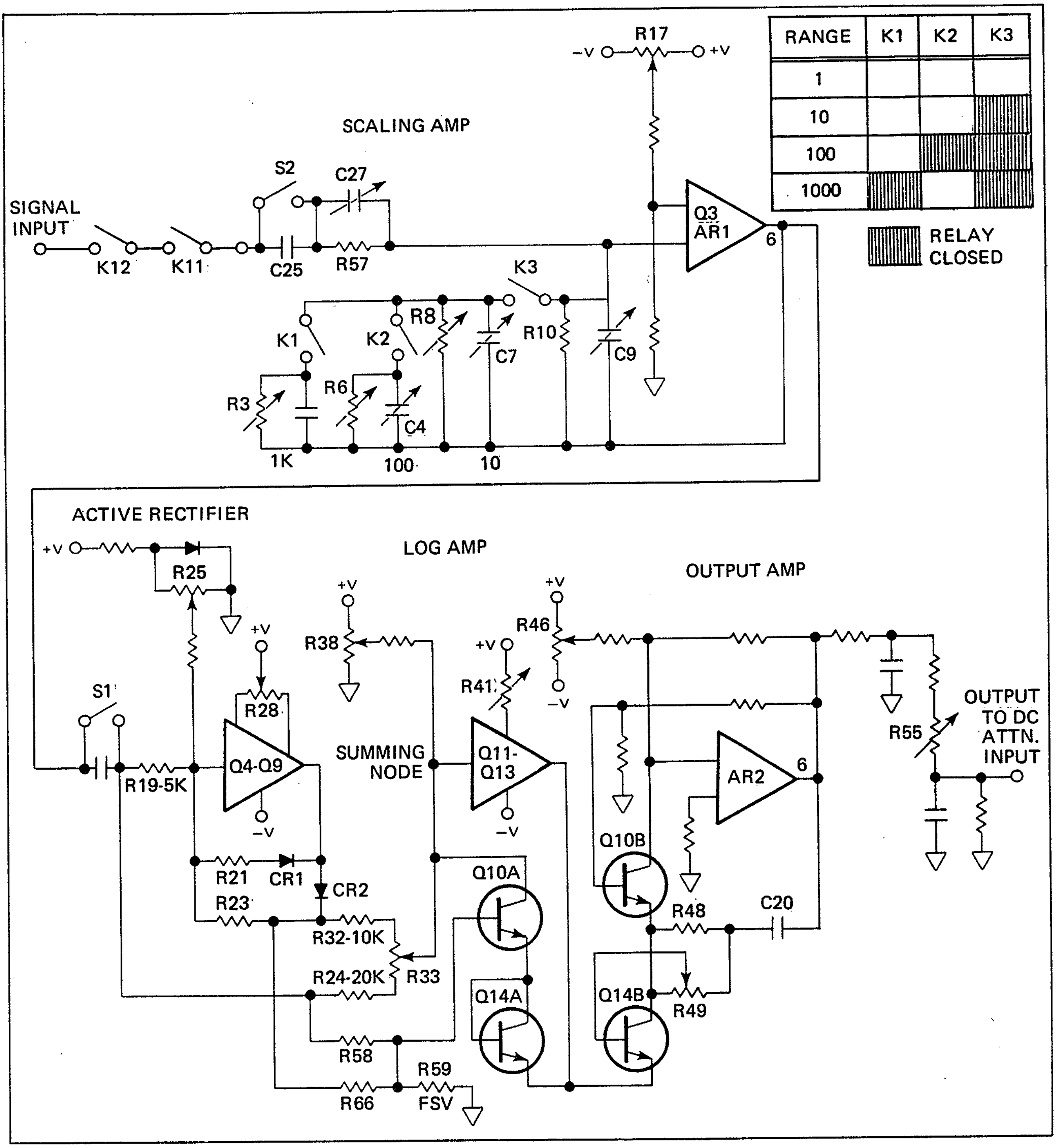


Figure 4.7 - RMS AC Converter

Q10, Voltage Reference VR1, and Opto-isolator drivers U9/U17. A simplified diagram of the Analog Processor and supporting external circuitry is shown in Figure 4.8 where designators and circled numbers relate to the A/D schematic at page 6-9. A block diagram of the A/D Digital Counter and Control is presented in Figure 4.9.

4.4.1.3 The A/D conversion is performed by two LSI circuits - a charge-balancing Analog Processor (U11) and a proprietary Digital counter and control IC (U10), that contains all the digital circuitry for the 'quantized feedback' system. The Analog Processor contains a bipolar comparator, bipolar integrating amplifier, buffer amplifiers and analog

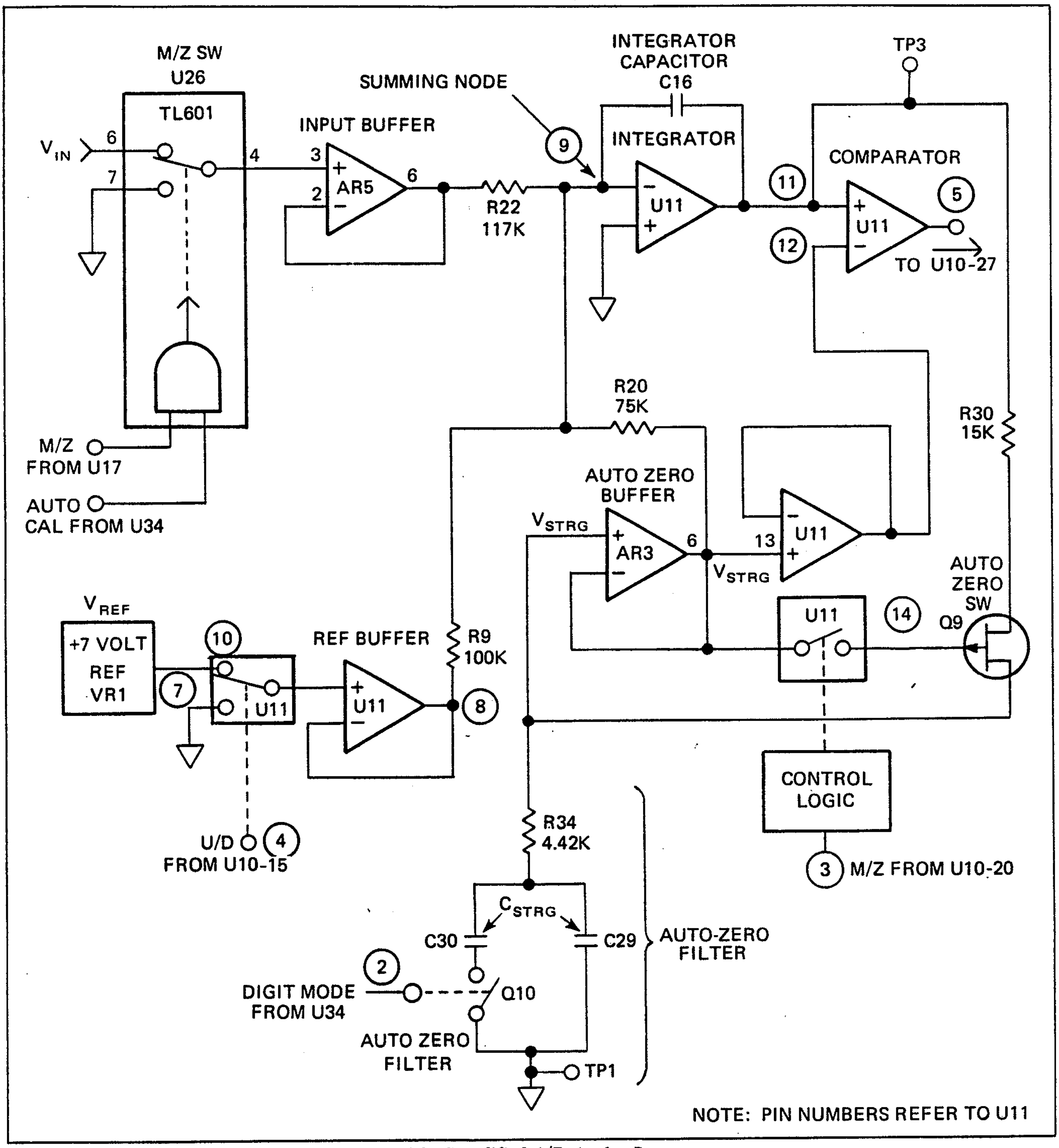


Figure 4.8 - Simplified A/D Analog Processor

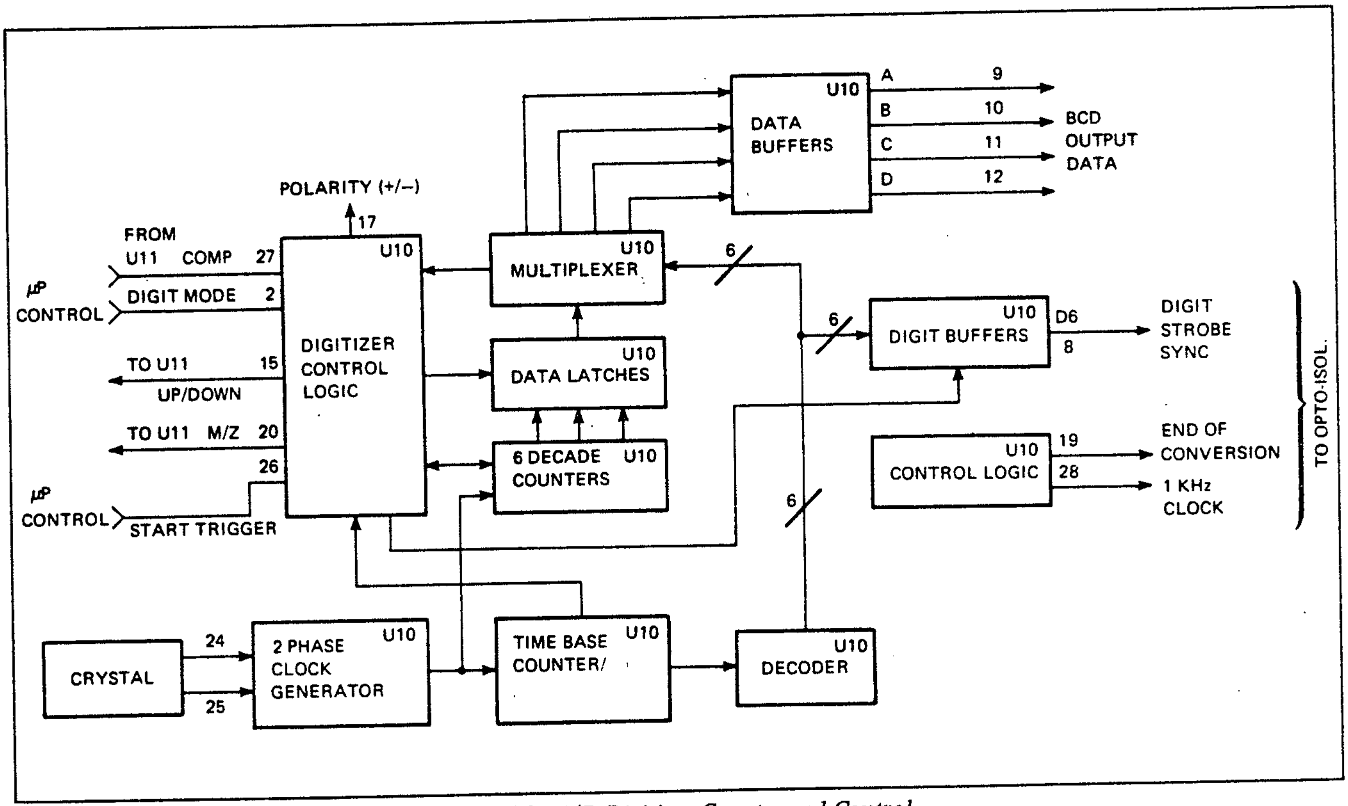


Figure 4.9 - A/D Digitizer Counter and Control

switches. External Buffer amplifiers AR5 and AR3, measure/zero (M/Z) switch U26 and auto-zero switch (Q9) are used to improve performance of the Analog Processor. The Digital Control I.C. is a synchronous digital processor and combines the time-base generation, counting, data multiplexing and random logic necessary to control the Analog Processor. A stable 7 volt reference voltage for the A/D converter is supplied by VR1.

4.4.2 Time Base Generation.

4.4.2.1 MEASURE/ZERO (M/Z) SIGNAL.

4.4.2.1.1 Basic timing signals for the A/D Converter are generated by the 2-Phase Clock Generator and Time-base Counter in U10. The Clock Generator, controlled by an external crystal, supplies a two-phase output at a 2.4576 MHz frequency (2.048 MHz in 50 Hz instruments) to the Time-base counter. In 60 Hz instruments operating in the 5-1/2 digit mode, the Time-base counter divides the clock frequency into sampling periods of 614,400 pulses (250 milliseconds). A period of 409,600 pulses (166.67 ms) is defined as the Measure Interval and 204,800 pulses (83.33 ms) as the Auto-zero interval. When operating in the 4-1/2 digit mode the Measure Interval is 16.67 ms and the Auto-zero period is 8.33 ms. The resulting measure/zero (M/Z) waveform, shown in Figure 4.10, is applied to the analog processor. When the logic level on the START TRIGGER line is held low, the M/Z waveform is generated continuously and the DMM is taking measurements continuously at a rate of 4 readings/sec (60 Hz instrument, 5-1/2 Digit mode) or 40 readings/sec (60 Hz instrument, 4-1/2 Digit mode). When operating the DMM in the Hold/Command (triggered reading) mode, a logic high on the START TRIGGER line holds the system in the Auto-zero mode. A negative going pulse on this line initiates one measurement cycle.

4.4.2.2 UP/DN CONTROL SIGNAL.

4.4.2.2.1 The up/down (U/D) control signal to the Analog Processor is also derived from the Time-base counter. This control signal has a period of 160 clock pulses. During the Auto-zero mode the U/D waveform has a 50% duty cycle (logic high for 80 counts and logic low for 80 counts). During the Measure interval the Digitizer Control logic examines the output of the comparator in the Analog Processor once each 160 clock pulses. If the comparator output is high, the UP/DN control will be high for 10 clock pulses and low for 150 clock pulses during the next 160 clock pulses. If the comparator output is low, the U/D control will be high for 150 pulses and low for 10 pulses. How the U/D control is used to control the Analog Processor is discussed in the following paragraphs.

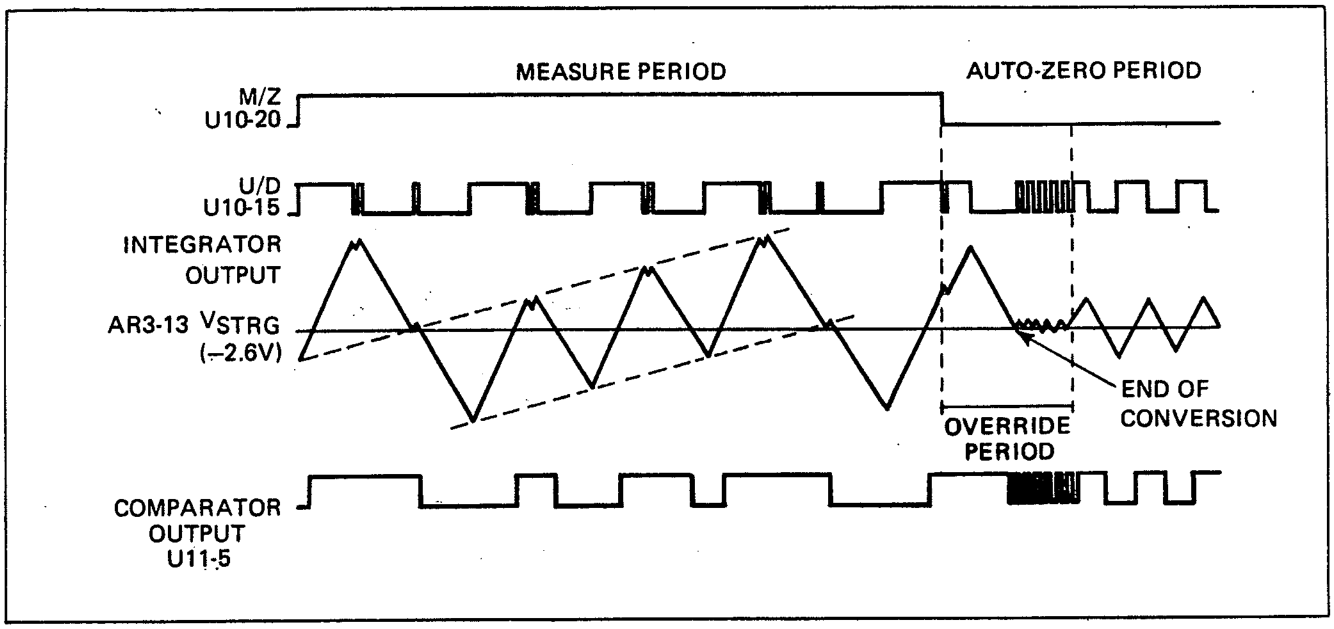


Figure 4.10 - Typical A/D Converter Waveforms

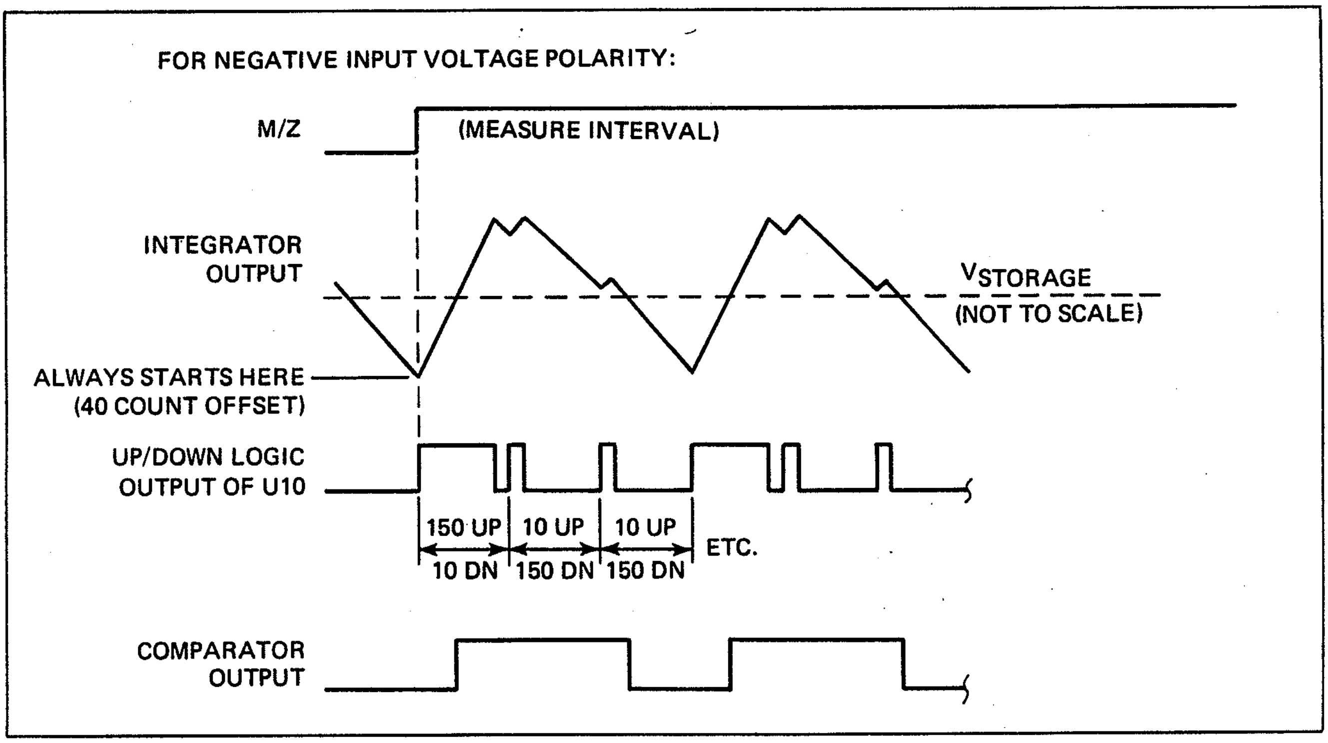


Figure 4.11 - Waveforms at Beginning of Measure Interval for Negative Input

4.4.3 Auto-Zero Interval.

4.4.3.1 Referring to Figure 4.8, during the Auto-zero (A/Z) interval the input of AR5 (Input Buffer) is switched from the Isolator output to analog common by M/Z switch U26. Auto-zero switch Q9 is enabled and connects the Integrator output to Auto-zero filter capacitors C29 and C30, and the input of Auto-zero buffer AR3. Both switches are controlled by the M/Z signal from the Digital Control IC, U10. The U/D control signal, with its 50% duty cycle, alternately switches the input of the Reference Buffer between Analog Common and the 7 volt reference, VR1. When the U/D control is low, the Reference Buffer output is equal to +7 volts; when the U/D control is high, the Reference Buffer output is zero. The Integrator input current (pin 9 of U11) is a summation of currents from the Input Buffer, Reference Buffer and Auto-Zero Buffer through resistors R22, R9 and R20 respectively. The average current through R9 is equal to one-half the Reference Voltage divided by the value of R9, $\left(\frac{VREF}{2R9}\right)$, because the reference current is flowing through R9 half of the time. The Auto-zero Buffer supplies a current through R20 equal to the voltage on the Auto-zero Filter capacitors divided by R20. The output of the Integrator is applied to the Auto Zero Filter capacitors C29 and C30 through R30, Q9 and R34, and the capacitors charge to a voltage proportional to the average value of the input currents (approx. −2.6V). This voltage is negative because of the inverting action of the Integrator. C29 stores the Integrator output in the 4-1/2 Digit mode, and C30 is switched in parallel by Q10 when the 5-1/2 Digit mode is selected to provide a longer time constant. Note that the voltage, Vstrg, at the output of AR3 is also applied to one input of the comparator through an internal Buffer Amplifier. This voltage remains on the comparator during the Measure Interval and establishes the comparator threshold at Vstrg (−2.6V).

4.4.3.2 The loop around the Integrator reaches equilibrium when the sum of the currents into the Integrator summing node equal zero. The voltage on the Filter capacitors (Cstrg) remains at approximately −2.6V when the Auto-zero switch Q9 opens at the end of the AZ interval because of the high input impedance of AR3. The BCD counters in U10 are also reset to zero by the last clock pulse of the Auto-Zero interval.

4.4.4 Measure Interval.

4.4.4.1 At the start of the Measure Interval; (a) the M/Z control goes high, switching the Isolator output to the Input Buffer AR5 through M/Z switch U26, (b) Auto-Zero switch Q9 is switched OFF, disconnecting the Integrator output from the Auto-Zero Filter capacitors, (c) U/D control is high, switching the Reference Buffer input to Analog Common, and (d) the Integrator output is slightly more negative than Vstrg (see Figure 4.11). At this time, the only inputs to the Integrator are Vstrg and the input signal from the Isolator (buffered by AR5). With only these two inputs, the Integrator output will always move in a positive going direction, independent of the polarity of the signal from the Isolator. As the Integrator output moves away from Vstrg, the comparator senses the output of the Integrator and compares it to Vstrg on the other Comparator input (pin 12 of U10). The comparator output transmits the sense of deviation of the Integrator output from Vstrg to the Control Logic circuits in U10. The Control Logic circuit generates the UP/DN control signal as described in paragraph 4.4.2.2 and shown in Figure 4.10 and 4.11. The effect of the two duty cycles (10 up, 150 down or 150 up, 10 down) is to source or sink a net 140 clock pulses of charge to integrator capacitor C16, thus driving the Integrator output toward Vstrg and accumulate a net 140 counts in the up/down counters. The charge is supplied by the current through R9 from the buffered Reference voltage. Charge is added to C16 when the Reference Voltage is applied to R20 and subtracted when the Reference voltage at the output of the Reference Buffer is zero. The net amount of charge required to keep the Integrator output at Vstrg during the Measure Interval is measured by the Up/Down Counter in the Digital I.C. The BCD count at the end of conversion equals the number of charge parcels necessary to cancel the input voltage and the resulting digital count is proportional to the analog voltage.

4.4.5 Over-Ride Interval.

4.4.5.1 At the end of the Measure Interval the total counts accumulated by the counter will be a multiple of 140. A residual voltage on Integrator capacitor C16 represents the remaining unresolved portion of the input. This voltage is cancelled and the corresponding counts accumulated during

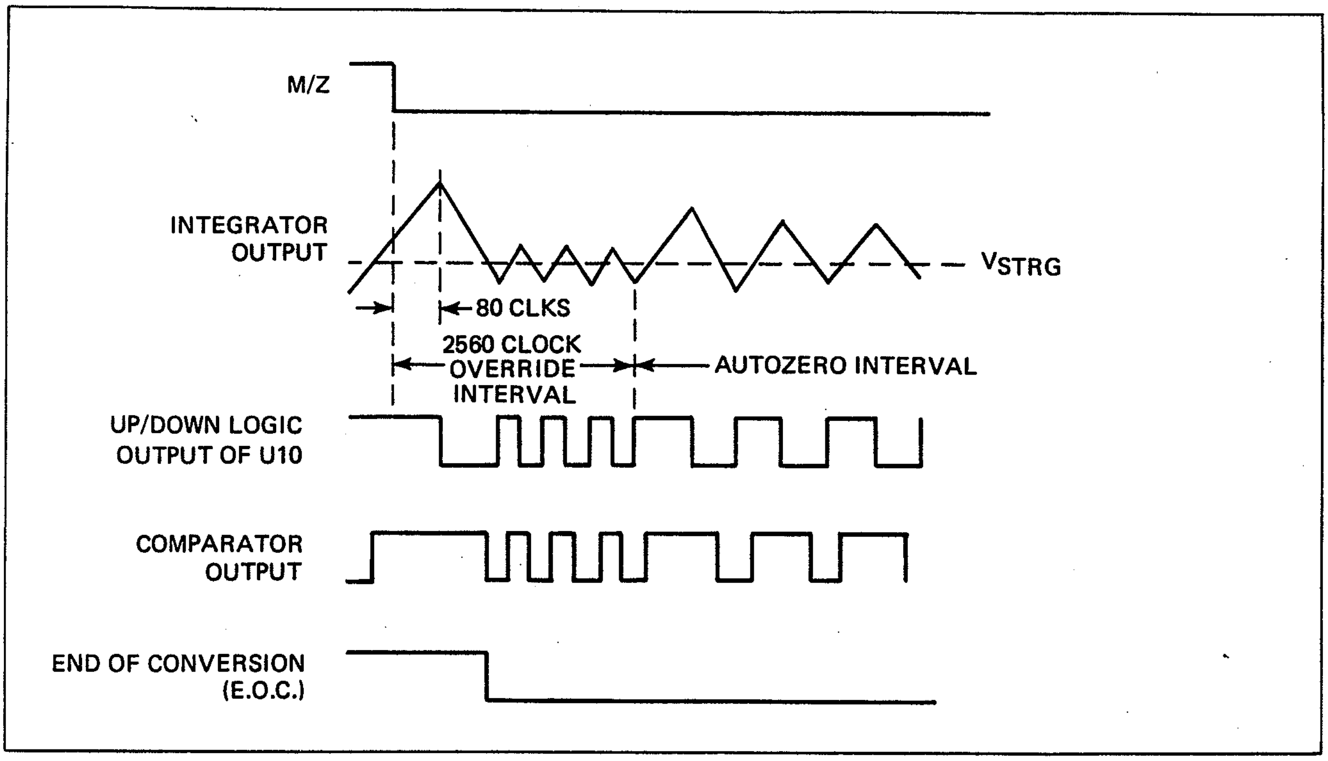


Figure 4.12A - Waveforms During Override Interval (Integrator Output More Positive Than V_{strg} At End of Measure Interval).

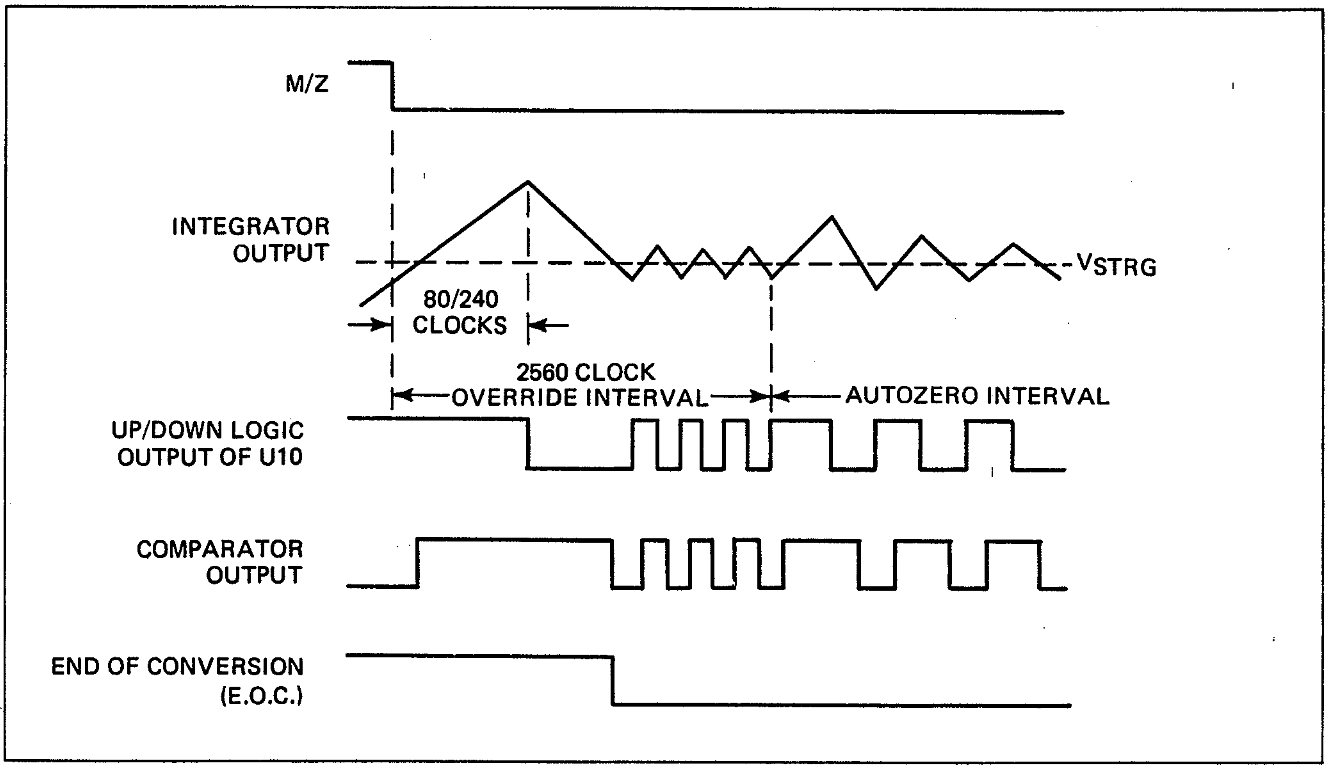


Figure 4.12B - Waveforms During Override Interval (Integrator Output More Negative Than V_{strg} At End of Measure Interval)

an interval at the beginning of Auto-Zero called the "Override Interval". The Override Interval is a fixed 2560 counts long (1.04 ms in a 60 Hz instrument). During the Override Interval the input of AR5 (Input Buffer) is switched to ground through M/Z switch U26, but the AZ Filter remains disconnected from the Integrator output (Q9 is OFF). When the Measure Interval ends, the Integrator output will be either higher or lower than Vstrg. Override Interval waveforms for both conditions are shown in Figure 4.12A and B.

4.4.6 Digitizer Counter & Control Output.

4.4.6.1 The 4 bit BCD data stored in the data latches of U10 are multiplexed and routed through the opto-isolator drivers U9 and U17, and presented one digit at a time to the microprocessor control section of the DMM.

4.4.6.2 The A/D output control signals are:

a) END OF CONVERSION: Advises μP that A/D conversion is completed and that a reading is ready.

b) 1 KHz: Synchronizes data transfer between A/D and μP.

c) DIGIT STROBE SYNC D6: Advises μP when the sixth BCD digit is being transmitted.

d) POLARITY: Polarity information passed on to the μP (+ or – input).

4.5 DIGITAL THEORY OF OPERATION.

4.5.1 Digital Hardware Description.

4.5.1.1 The DMM's digital control centers around U35, (Dwg. on page 6-10), a 6802 microprocessor which executes the program contained in ROMs, reads data from various locations throughout the DMM and stores data to RAM and to various hardware locations throughout the DMM. The microprocessor executes the ROM program based on these data, performs calculations, and makes decisions to control all the functions described in Section 3 of this manual.

4.5.1.2 The hardware locations contributing data to the microprocessor are the Digitizer (via opto-couplers OCI1 and OCI2), the keyboard on the front panel, and through the GPIA (U44) which passes commands from the 488 bus to the μP. This group is located at Sections 6, 7, 8 and 9 as shown in Figure 4.1.

4.5.1.3 In turn, the microprocessor outputs processed data to the GPIA and LED display. The μP also sends control information to the Digitizer and the analog hardware via opto-isolator OCI3. The Figure 4.13 graphically presents the hardware network controlled by the microprocessor. The schematic drawing on page 6-11 listed in Section 6 presents the coded designators that input and output to/from the microprocessor through the opto couplers.

4.5.2 The Microprocessor Section.

4.5.2.1 The microprocessor section (MPU) located in Section 6 on the motherboard consists of the microprocessor U35, with program memory IC's U27, U28, U29 and U30, address decoders U14 and U15, interrupt control hardware U2, U6 and U20, and non-volatile memory system U43, U42, VR12, BT1 and Q21. The complete schematic drawing is listed in section six pages 6-10 and 6-13.

4.5.2.2 When power is first applied to the microprocessor (μP), the R76-C75 time constant on the μP's RESET input (U35-40) holds the μP in reset long enough for the power supplies and clock to stabilize, then reset goes high (HI) enabling the start-up routine.

4.5.2.3 The DMM system clock is generated by the μP combining internal components with external components connected to pin U35-38 and U35-39 comprising of a 3.579 MHz crystal Y1 and C73-C76 components. The μP divides this frequency by four then outputs at pins U35-37 as 'E' the system clock of 895 KHz (approx.) for all μP bus components.

4.5.3 Program Memory.

4.5.3.1 The entire program memory for the μP resides in ROM's U27 through U30. IC's U27, U29, U28 and U30 are connected so that each can hold a 2Kx8 model 2716 EPROM or U29 and U30 can be omitted and U27 and U28 can each contain a 4Kx8 ROM. The μP directs other hardware locations dedicated to specific memory assignments as the Non-Volatile-Memory; GPIA and Digitizer.

4.5.4 Address Decoding.

4.5.4.1 The IC's U14 and U15 comprise the address decoding hardware used by the μP. The inputs to the address decoders are various address lines from the μP as well as other control lines. Each decoder has 8 normally high outputs, AY0 to AY7 and BY0 to BY7 which are used as 'Chip selects' for various hardware throughout the DMM. When the μP places an address on its address bus, U14 and/or U15 decode this address and supply the required chip select to the selected component which is being addressed by the μP.

4.5.4.2 The outputs of U14 are not gated internally with the clock, therefore the negative pulse widths may vary from 900 to 1200 ns. The outputs from U15 are internally gated

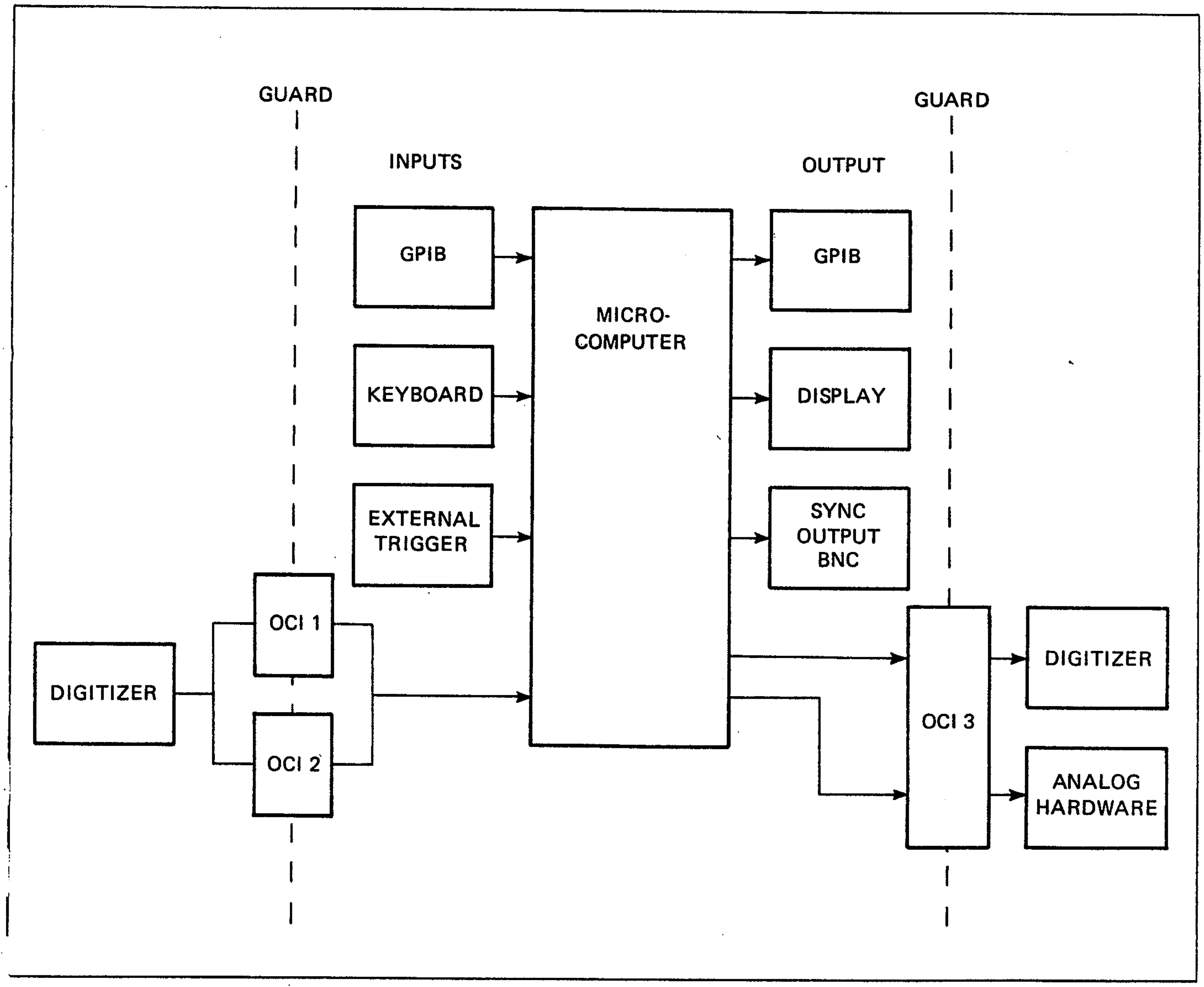


Figure 4.13 - Main Inputs To And Outputs From The Microcomputer

with the system clock E, therefore the outputs are practically a consistent pulse of 516 ns.

4.5.5 Non-Volatile Memory.

4.5.5.1 The DMM uses a non-volatile memory (NVM) to store calibration (CAL) constants for later recall. The constants are stored during laboratory calibration and are recalled from the NVM whenever the DMM Function or Range is modified. The NVM is comprised of U43, a CMOS RAM, and Nand gate U42 along with a three volt lithium battery BT1, zener diode VR12, a constant current regulator Q21 and steering diodes CR17 and CR21.

4.5.5.2 NVM POWER SUPPLY

4.5.5.2.1 During normal DMM power-on operation, the NVM circuit receives +9 volts unregulated from the digital power supply. The current from the unregulated supply is regulated by Q21, a FET connected as a constant current source. This constant current (normally 7-13 ma) flows to ground through VR12, creating a stable + 5.6 volts at the anode of CR17. This + 5.6 volts causes CR17 to forward bias, and supplies approximately + 5 volts to the anode of CR21, to the Vcc connection, and to IC's U42 and U43. The presence of + 5 volts on CR21's cathode causes it to turn off, thus preventing battery charging.

4.5.5.2.2 During the AC power-off periods, battery BT1 causes CR21 to forward bias so that approximately 2.5 volts is available to power U42 and RAM U43. This same voltage reverse-biases CR17 which prohibits battery flow into the power supply.

4.5.5.3 NVM WRITE-PROTECT

4.5.5.3.1 A hardware Write-Protect circuit prevents accidental modification of the contents of RAM U43 during normal power-up operation. This circuit is comprised of R/W control gate U42, a 10K pull-up resistor R79 and CAL-switch S1 which is located behind the front panel, refer to Figure 3.1-54 for illustration. When the switch is open, pin 14 on RAM U43 constantly remains HI, which prevents any RAM "write" operation so that its contents cannot be modified. When the CAL switch is depressed, the μP can drive the WRITE pin on the RAM LO, enabling the U43 memory modification.

4.5.5.4 NVM POWER-DOWN PROTECT

4.5.5.4.1 A power-down to deselect circuit prevents loss of RAM U43 CAL constants during power-up, power-down, and power brown-outs. The circuit is comprised of U53, a voltage level detector, along with the voltage-divider resistors R85 and R86.

4.5.5.4.2 U53 is configured to detect voltage variations in the + 5 VA power supply. During power turn-on, the + 5 VA supply passes up through the + 4 volt level, causing the voltage at U53 pin 3 to pass through approximately 1.2 volts. When this occurs, U53 pin 4 switches from the "off" state and becomes a low resistance path to ground, causing a logical low at U42 pins 3, 4 and 5. U42 pin 6 then goes high, allowing chip-select pulses from the μP to proceed thru to U43 pin 1. When power is cycled off or a brown-out occurs, the voltage at U53 pin 2 falls below 1.2 volts and a logical low appears at U42 pin 6, thereby blocking any further chip select signals

4.5.6 Interrupt Control Hardware.

4.5.6.1 The interrupt signals to the μP are processed by the interrupt control hardware consisting of dual Flip-Flop U2, two NAND gates in U6, and 1/6th of inverter U7.

4.5.6.2 The interrupts from the Digitizer and GPIA are NANDED by U6-4, 5, 6 and inverted by U7-3, 4, to appear on the interrupt request (IRQ) pin of the μP U35-4. This ANDing either from the Digitizer via the lower half of U2 or an interrupt from the GPIA via pin U6-5 will cause an interrupt to be gated to the μP.

4.5.6.3 External Triggers from the rear panel BNC connector J202, drive pin U6-2 LO then are inverted by U6 causing a positive edge at pin U2-3. This trigger clocks a LO at pin U2-5 which will cause a non-maskable interrupt (NMI) to occur at the μP pin U35-6. This NMI will cause the μP to cease its present software calculations and act upon the external trigger. The number of triggers arriving at the μP determine whether the μP will re-enable the external trigger or not. Enabling the external trigger occurs by the μP pulling pin U2-4 LO momentarily. If this is done, that portion of U2 will be set so that a second external trigger can be received by the hardware. If this is not done by the μP as would be the case when many external triggers are received rapidly, then pin U2-5 will remain in a LO state until the μP decides to pull pin U2-4 momentarily LO to set that half of U2.

4.5.6.4 The Analog Interrupts which originate from the analog side of the DMM are used to clock the lower half of U2. These evenly timed interrupts occur every 6 ms (every 7.2 ms in 50 Hz DMM) and clock the lower half of U2 at pin 11. This causes pin U2-9 to go LO, which causes the μP's IRQ input to go LO. When the μP responds to this interrupt, it reads the output of U20, a hex three-state buffer. Since pin U2-9 is connected to pin U20-10, the μP can determine if the IRQ originated from U2 by examining the D7 output (pin 9) from U20. If U2-9 is found to be low, the μP applies a negative pulse to pin U2-10, which removes the IRQ.

4.5.6.5 The interrupts which occur approximately every 6 ms as a result of the clock on pin U2-11 are used by the μP to sequence the scanning of the keyboard and to check whether certain front panel LED's need up-dating. If problems are observed in any of these areas, then a correct clock into pin U2-11 should be verified.

4.5.7 The Hardware Control Codes.

4.5.7.1 The hardware which brings information from the analog section of the DMM to the digital section is presented in schematic drawing on page 6-11.

4.5.7.2 The eight signals entering from the left edge of schematic on page 6-11 are brought in from the analog section of DMM through the opto-isolator couplers OCI-1 and OCI-2 to the digital three-state hex buffer U16. Four of these are multiplexed (MUX) BCD data lines A, B, C, D lines. Via these lines, 6 digit MUX BCD data is brought across guard through the opto-isolators. The other four lines are single lines designated as follows:

a) POLARITY: This line indicates the polarity of the most recently completed reading.

b) 1 KHz: This lines supplies a 1 KHz frequency (0.833 KHz in 50 Hz DMM). The high-low transitions of the 1 KHz waveform are monitored by the μP to determine when a new BCD digit is being MUX across guard on the A, B, C, D lines.

c) DIGIT STROBE SYNC D6: This line is used to generate real-time interrupts to the μP which was described previously and to help MUX the sign (polarity) bit into the μP.

d) EOC: (END OF CONVERSION) This line changes state when a new reading has been completed. After crossing guard the EOC line is buffered by TTL Schmitt inverter (sections of U7) and is used to clock the input of the dual F/F at pin U8-11. When the F/F is clocked, the output pin U8-9 goes HI. This high output is read by the μP and indicates to the μP that a new reading is ready. The buffered output of the opto-isolator also goes, via U7 and U6 TTL buffer, to the display board and is used to drive the "sample" LED. Refer to Figure 3.1-56 for the sample LED location.

4.5.7.3 When operating on 5 1/2 digit mode, the μP spends considerable time waiting for a new reading to become available for process and display. It determines when a new reading is available by reading pin U8-9 via U13, the keyboard three-state hex buffer. When the μP reads U13-3 HI, it then knows that a new reading is available and it begins to read the six digits which are constantly MUX across guard through opto coupler OCI-2. The μP reads the MUX BCD pulses and other control lines through U16 a three-state hex buffer.

4.5.7.4 A typical set of waveforms are presented in Figure 4.14 as they would appear to the μP while reading the MUX BCD data from the analog section, crossing guard, to the input of U16. The μP uses the positive edge of the 1 KHz signal to indicate when it should read the next nibble of BCD data from U16 inputs. The μP uses the DIGIT STROBE SYNC D6 signal to indicate when the most significant digit is MUX across guard.

4.5.7.5 The LO DIGIT STROBE SYNC D6 signal also causes the "sign" bit to be substituted in place of the D bit at U16's input. This switching of the sign bit in place of the D bit is done via the wired OR connection between the open collector outputs of OCI2 pin 10 and OCI1 pin 15.

4.5.8 Analog Control Registers.

4.5.8.1 The analog control hardware is housed in sections 4, 5, and 6 on the motherboard. The principal schematic on page 6-8 presents a relay operation chart and circuit details. Outguard portions of the circuit are shown on page 6-11.

4.5.8.2 The analog control system is comprised of a 4 bit latch U32, two shift registers U33 and U34, two relay drivers U18 and U19, relays K1 through K13, Schmitt trigger U25 and fet driver U36, as shown in Figure 4.15.

4.5.8.3 The μP program controls the digitizer, function, and range relays through 3 registers, 2 of which U34 and U33 are located on the analog side of guard, with the third U32, located on the digital side of guard.

4.5.8.4 U32 is a 4 bit latch which is loaded from the μP's data and address bus. The output from U32 is used to load registers U34 and U33 as well as trigger the digitizer shown on schematic on page 6-9.

4.5.8.5 U34/U33 REGISTER LOAD.

4.5.8.5.1 The DMM's function, range and/or integrate time can be modified as a result of keyboard inputs, GPIB commands, or autorange. When this occurs, a new relay drive bit pattern is determined by the μP. This pattern is then shifted across guard one bit at a time. The timing of the drive bit pattern is shown in Figure 4-16, the Register Load Timing diagram.

4.5.8.5.2 The first bit of this pattern, along with other control signals is latched into U32 from the μP's data bus and address bus. After propagating through the relatively slow opto coupler OCI-3, the data bit appears at the 'D' input of U34, along with a LO signal at U34's clock input. The microprocessor then stores the first bit to U32 along with other control signals that after progating through the opto-coupler, the first data bit remains at U34's 'D' input along with a "HI" signal at U34's clock input, which causes the first data bit to be shifted into U34. The above sequence is repeated until all 16 bits have been shifted into U34 and U33, which requires about 20 milliseconds.

4.5.8.5.3 After shifting all 16 bits into U34 and U33 the μP then strobes the shifted bits into the output registers of U34 and U33. To do this the μP stores a control bit pattern to U32 which propagates through OCI-3 and places a high level on U34-1 and U33-1. About 2 ms later, the μP removes this signal.

4.5.8.5.4 The output bits from U34 and U33 then energize relays via the open collector drivers U18 and U19, control Isolator gain via U36, or control the digitizer.

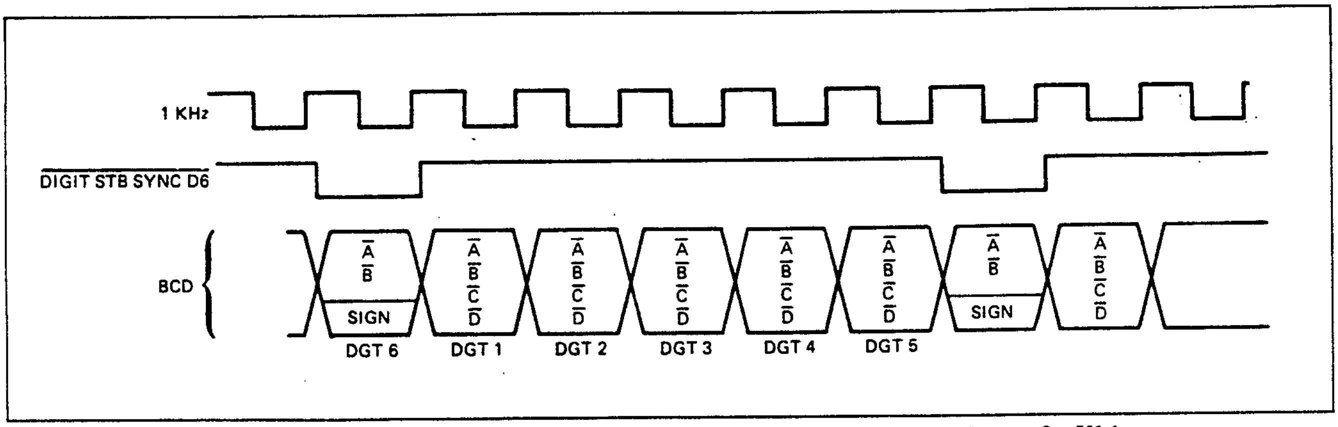


Figure 4.14 - Typical Waveforms From Across Guard As Seen By μP Via Inputs On U16

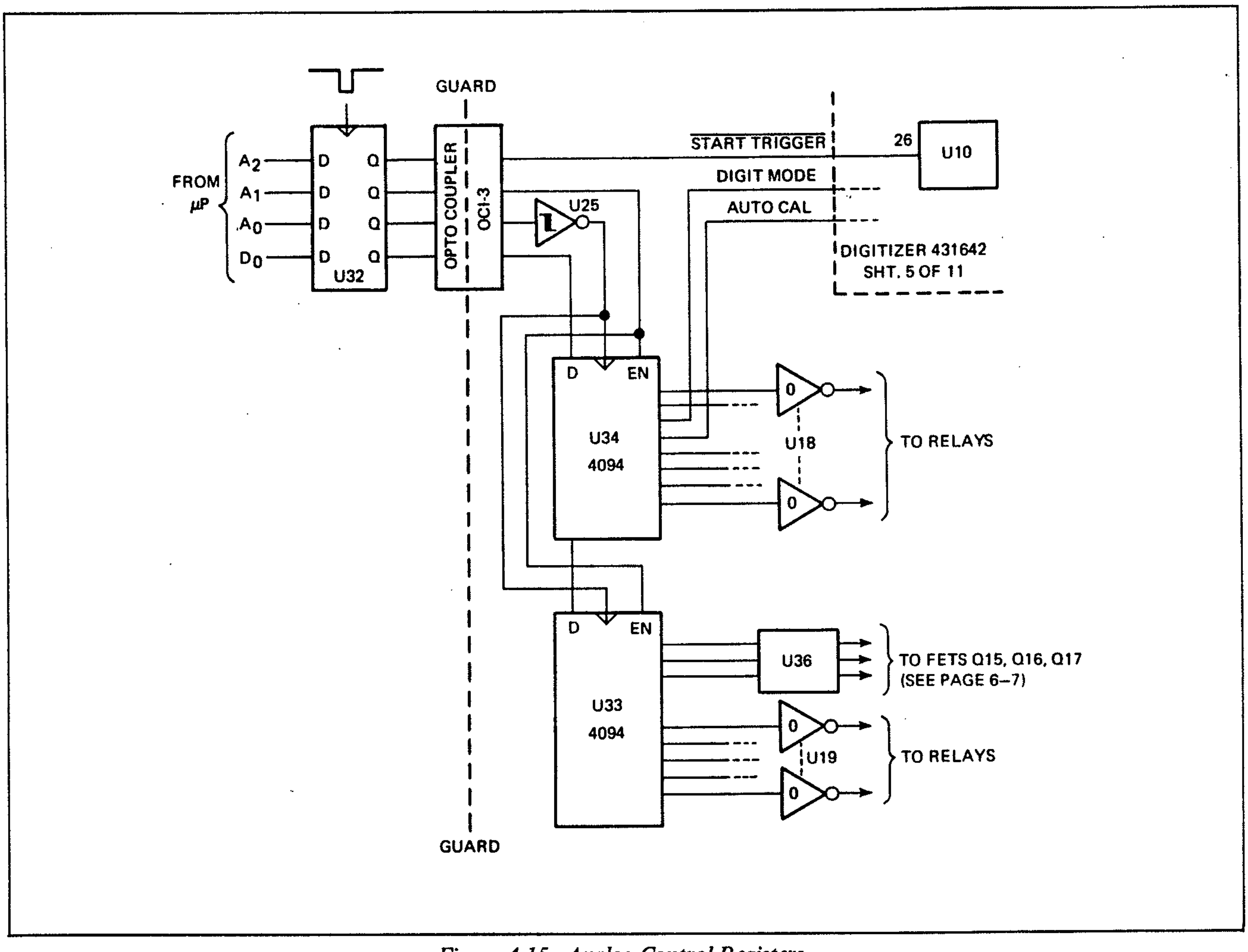


Figure 4.15 - Analog Control Registers

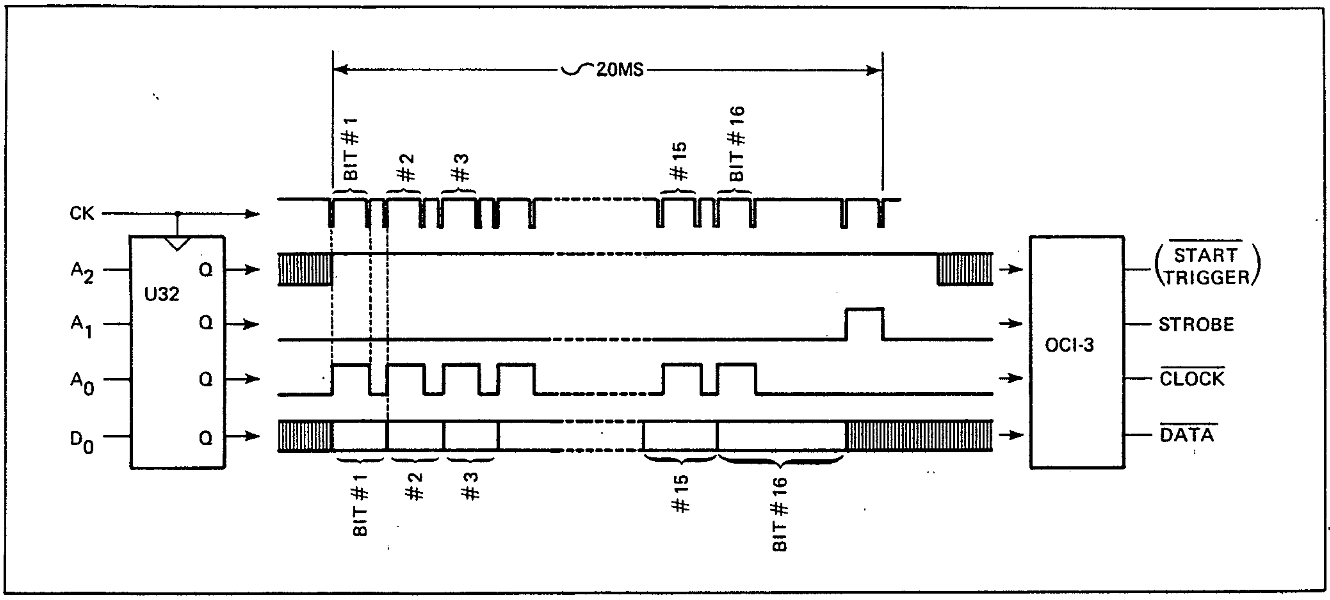


Figure 4.16 - Register Load Simplified Timing Diagram

4.5.8.6 DIGITIZER TRIGGERING.

4.5.8.6.1 When the μP requires a reading, it loads U32 with address line A2 LO. This then appears at U32's output, propagates across guard, and places a low level on pin 26 of U10 (digitizer drawing on page 6-9) to cause a read cycle.

4.5.8.6.2 When in the hold mode and at other times, the microprocessor waits for verification of a digitizer trigger by watching for a LO on pin 10 of U13, the keyboard buffer on page 6-14.

4.5.8.6.3 When operating in the "track" mode, (internal trigger) the μP leaves a LO on U10 pin 26 almost all the time in order to cause continuous triggers.

4.5.9 Keyboard Theory of Operation.

4.5.9.1 The DMM's keyboard is located on the display PCB whereas the associated ICs located on the motherboard; referred to as section 4 on the sectional chassis layout and detailed on schematic drawings on pages 6-14 and 6-17.

4.5.9.2 The keyboard circuitry consists of MB-U5, an open-collector inverter used to buffer the μP's address lines which drive the N, M, L, H, K, and J columns of the keyboard. The keyboard buffer U13 is a three-state buffer connected so that the μP can read the signal from the keyboard rows T, R, U, and S. The pull-up resistor network Z2 pins 3 through 6 ensures that the μP will read a HI from U13 if its inputs become open, a condition that exists when no key is pressed. The chip select for U13 is DSPE, which is the same chip select for U12. This chip select originates from the NAND gate output U6-8. See paragraph 4.6.3.1 for further explanation.

4.5.9.3 The OPERATION is described as follows. When the μP must determine if any key is pressed, it reads from U13 while address lines A0-A5 are high. The ones on A0-A5 lines propagate through U5 and appear as zeros on N, M, L, H, K and J columns of the keyboard as shown in Figure 4-14. When a key is pressed, the μP will read a zero on one of the row outputs through U13, the remaining rows will read ones. When a zero does appear, the μP then scans each keyboard column one-at-a-time by reading from U13 with only one of the lines A0-A5 high and others low, until the proper column has been driven low, and that a zero once again appears in the read from U13. Once this occurs, the μP suspends further keyboard scanning and processes the key in software.

4.6 DISPLAY BOARD.

4.6.1 Display Hardware.

4.6.1.1 The display hardware is configured on the motherboard (MB) as well as on the display board (Dspe). The LSI Display Controller and Driver MB-U12, 6-bit Range Latch MB-UI are located on the motherboard (MB). The display PCB contains the 7-segment LED read-outs DS1 through DS7. Function-Range-Status LEDs brightness-control current-limiting resistors and display drives V1, V2, and V3. This group occupies section 9 on the chassis.

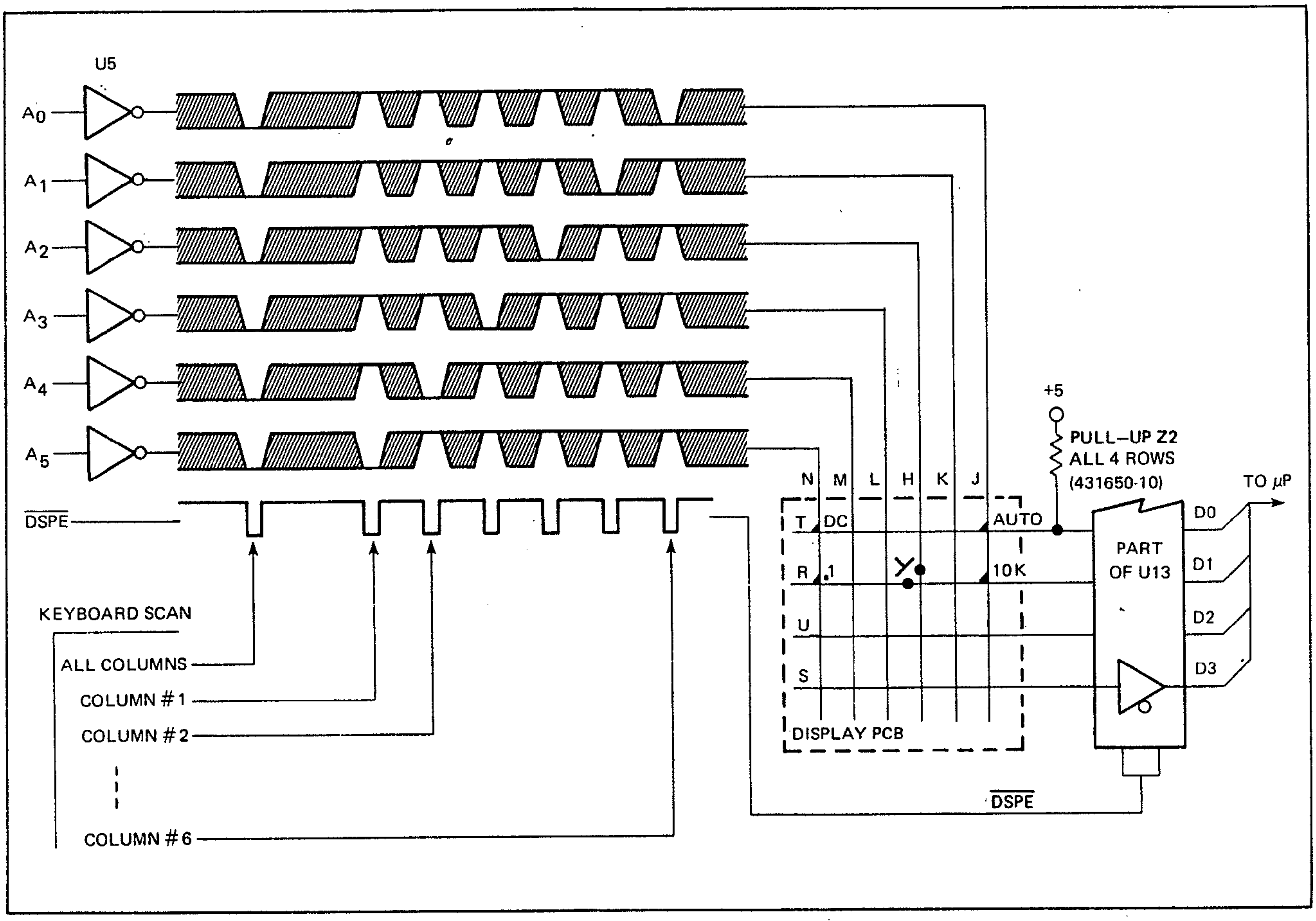


Figure 4.17 - Keyboard Block and Timing Diagram

4.6.2 Display Description.

4.6.2.1 The front panel LEDs are controlled by MB-U12 and MB-U1 through the μP. MB-U1 is a 6-bit latch which is loaded from the data bus by the μP. The outputs of MB-UI drive 5 range annunciator LED's and the "EXT REF" LED. The display configuration is presented in the block diagram Figure 4.18. This drawing merges the motherboard and display board components to give an overview of the display schematics on page 6-14 and the display control schematic on page 6-17.

4.6.2.2 The display device MB-U12 is an LS1 display controller with digit and segment drivers that execute the μP's LED bit pattern strobed through the multiplex scan circuitry. Dspe-U1 is a current sourcing driver which is used to buffer the display controllers column driver in the digit scan sequence. Dspe U2/U3 with associated resistors are current-sinking row drivers. The resistors R1 to R8 set the brightness level of the 7-segment and annunciator LEDs.

4.6.3 Operation.

4.6.3.1 The display controller shares a chip-select signal with the keyboard hardware. The AY2 output from the μP's address decoder U14 is effectively ORed with the μP's clock via pins U7-5/6 and pins U6-8/9/10, the resulting signal is called DSPE. This chip select is supplied as the negative read strobe to the keyboard and the negative write strobe to the display controller.

4.6.3.2 Whenever the μP wishes to update the LED pattern controlled by MB-U12, it latches a string of bytes into MB-U12 from the μP's address bus. The first of these is a byte which notifies the display controller that 8 data bytes will follow. The display controller differentiates between status bytes and data bytes by sampling the A8 address line during each write cycle (U12-9), which is high during status bytes and low during data byte writes. See Figure 4.19 for a simplified timing diagram.

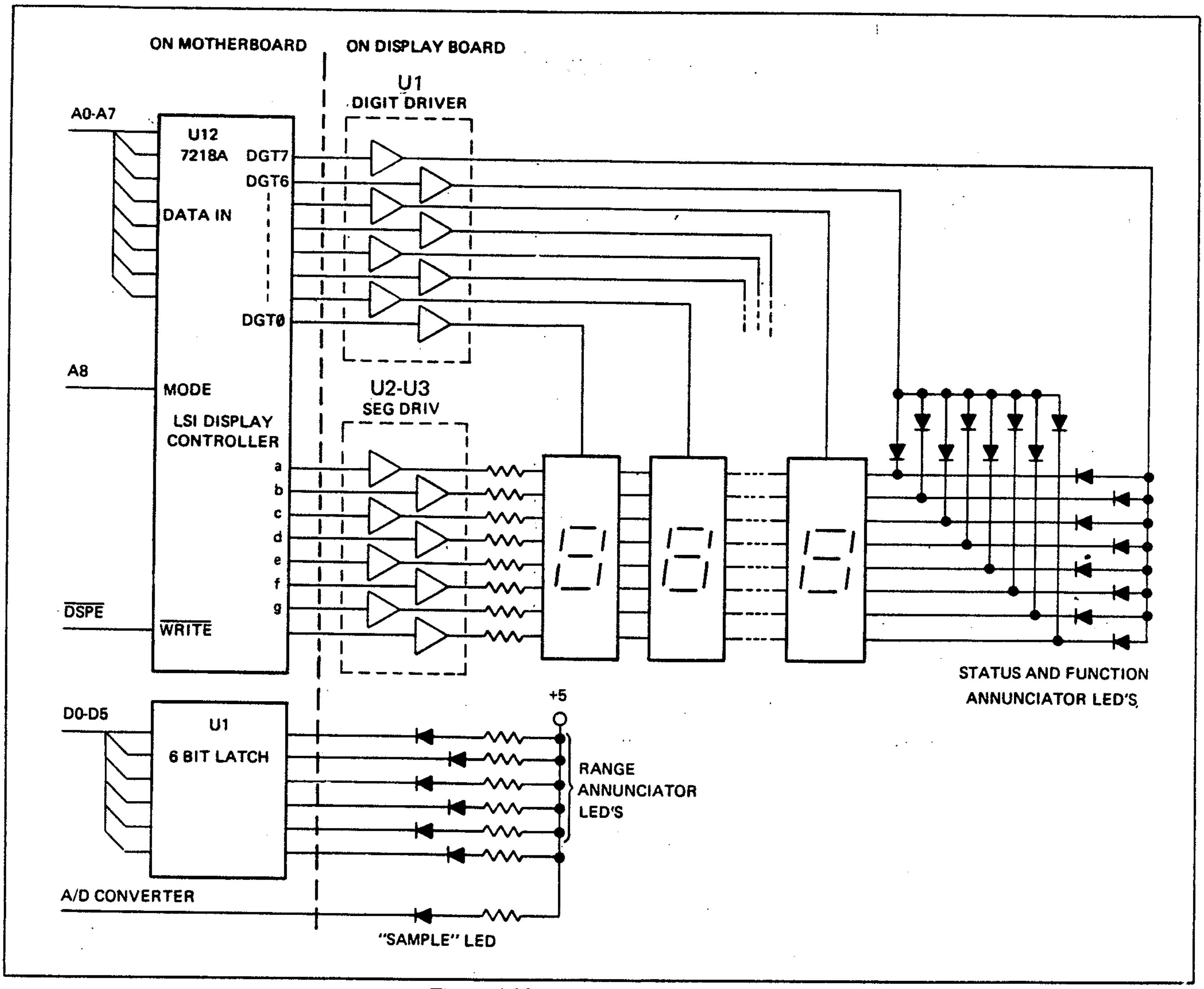


Figure 4.18 - LED Display Hardware

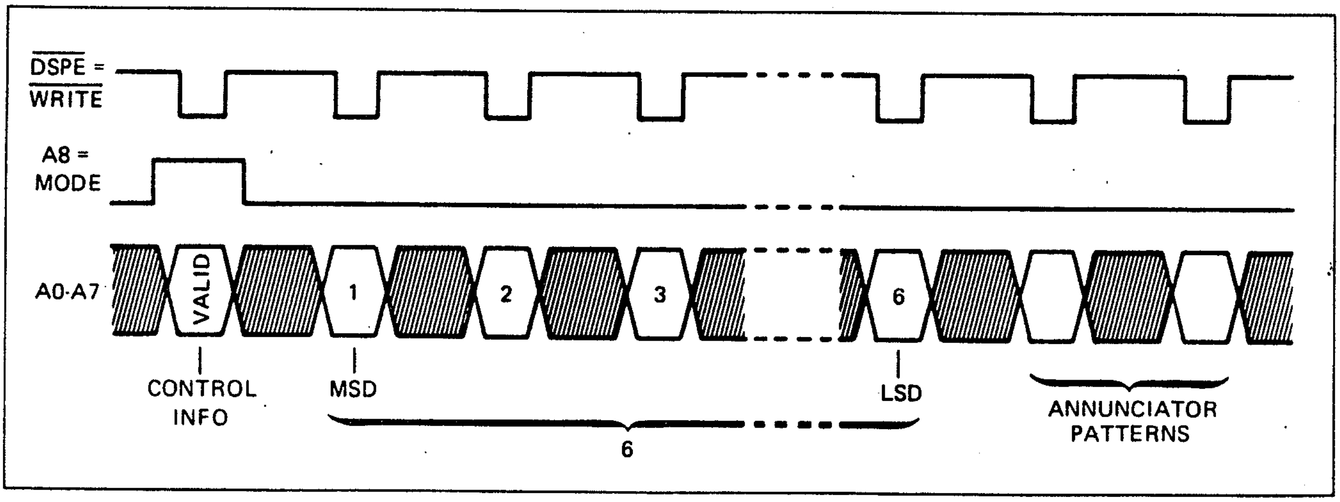


Figure 4.19 - µP Storage To LSI Display Controller Timing Signals

4.6.3.3 After all 8 data bytes have been latched into the display controller, it begins to refresh the 7-segment and annunciator LED's. To do this, the display controller first supplies an excitation MUX pattern to its row driver outputs a-g, which are buffered by DSPE U2/U3 and appear at the cathodes of all LED's. The display controller then turns on one column driver which, after being buffered by DSPE-U1, lights the appropriate LED's in that column. After a fraction of a millisecond, the controller turns off the column driver, changes the row excitation pattern, and turns on the next column driver, and so on. The LED refresh rate is fast enough that the human eye cannot detect the flicker.

4.6.3.4 The "Sample" LED located at the lower left corner of the decimal display is not controlled by U12 but instead, receives its control from the analog side of the instrument via U6-11 on page 6-11.

4.6.3.5 The brightness level for the Range LED's is set by the resistor network Z1 on the display PCB.

4.7 GPIB INTERFACE: THEORY OF OPERATION.

4.7.1 The DMM's IEEE-488 interface is centered around U44, the 68488 GPIA and positioned in section 8 on the motherboard. The other interface hardware in the GPIB Interface system include U46 and U47 bi-directional buffer/drivers; U37, U38 and U39 the Serial Poll Disable decoder; U45 the GPIA address switch buffer; and U40, U41 and U39 GPIA output holdoff circuit. These devices provide talker/listener capabilities, most interface commands and handle serial poll status bytes. The schematic for the GPIB hardware is listed on page 6-12.

4.7.2 The GPIA interfaces to the GPIB bus via U46 and U47 which are bidirectional octal GPIB transceivers. The U46/U47 data direction signal is controlled by the GPIA transmit/receive (T/R2) signal, from pin U44-27. The GPIA interfaces to the µP through 14 registers inside the GPIA which are accessed over the µP's data bus via GPIA pins U44-7 through U44-14.

4.7.3 The microprocessor's address and read/write lines are connected to the GPIA pins 37, 38, 39 and 5 to allow selection of the appropriate internal register by the µP. If the µP reads from the GPIA's register 4, the GPIA will not output data to the µP and will instead drive pin U44-4 low momentarily which will cause U45 to output the address switch setting to the microprocessor.

4.7.4 The GPIA handshakes most in-coming interface messages from the controller and acts upon them without disturbing the µP. If and when an incoming message or data byte requires a response from the µP, the GPIA drives its pin U44-40 low which sends an interrupt request IRQ to the µP via the interrupt control gate U6, which was previously discussed in paragraph 4.5.6. The µP then examines the GPIA's internal registers to release the IRQ and to determine the cause of the interrupt. The same interrupt sequence takes place if the GPIA is made a talker and has no byte to output.

4.7.5 The GPIB "Output Holdoff Circuit" was added between GPIA pin U44-18 and transceiver pin U47-7 to allow the µP more complete control to out-going bytes. This holdoff circuit has no effect except when the DMM is a talker, at which time it is used to pace the output of data and serial poll status bytes.

4.7.6 The GPIB Output Holdoff Circuit contains a 2-bit latch U40. The upper half of U40 is used to affect the output of all bytes while the lower half of U40 is dedicated to controlling the output of serial poll status bytes. U41 is a quad analog switch connected to U39 so that U40 is either enabling the passage of signals between pin U44-18 and pin U47-7 or U41 is forcing a zero on pin U44-18 to make the GPIA believe that no other 488-bus devices are ready for data.

4.7.7 The ICs U37, U38 and U39 pins 3 to 6 are used to decode the interface message "SPD" (Serial Poll Disable = hex 18) but since data on the bus is inverted, the logic must decode the complement of the SPD message. The output from this logic is OR'd with the single line GPIB message IFC (interface clear), inverted and supplied as the reset input to pin U40-13 so that pin U40-8 will be set back to its normal high state after a serial poll has been completed.

5.1 SCOPE.

5.1.1 The maintenance section includes specification checks, calibration procedures, and troubleshooting data required for routine service. Voltage measurements with waveforms tabulated under performance tests are supplied for troubleshooting guidance. A suggested equipment list is covered in Table 5.1. In addition, the program error message list is included with general troubleshooting information. The parts locator shown in Figure 5.4 is a reproduction of the PCB. All component references throughout the Maintenance Section are plainly noted on this drawing.

5.2 SPECIFICATION CHECK.

5.2.1 Scope.

5.2.1.1 This section contains procedures that compare the operation of the instrument against the published specifications presented at the front of this manual. It is intended to be used for incoming inspection and as a periodic check to determine if the calibration of the instrument meets published specifications. The procedures provide sufficient checks to verify proper operation and that the instrument is within the 6 month accuracy limits. The required ambient temperature of the environment is 23 ± 5 degrees centigrade.

5.2.2 Required Equipment.

5.2.2.1 A list of equipment is given in Table 5.1. The specific types of equipment suggested are listed under the Suggested Equipment heading. This list provides a guide for selecting suitable equipment having characteristics equal to or better than the items listed.

5.2.3 DC Voltage Sources.

5.2.3.1 To produce voltage levels of necessary accuracy, special techniques are required. Suitable methods of generating these voltages are shown in Figure 5.1. Tables 5.2 and 5.3. A precise and traceable source of 10 volts is required, not only for calibrating the 10 volt range, but

Table 5.1 - Required Equipment

Function	Qty	Item	Minimum Use Specifications	Suggested Equipment
DC	(1)	Saturated Standard Cell Bank (6 cells)	1 ppm, certified	EPPLEY 106
	(2)	DC Voltages Sources	0.1 ppm resolution	FLUKE 332B
	(2)	Voltage Dividers, Adjustable	< 1 ppm linearity	FLUKE 720A
	(1)	Decade Resistance Box		ESI DB62
	(2)	Null Detector/μ Voltmeters	1 μV sensitivity	FLUKE 845AR
AC	(1)	Thermal Transfer Standard	50 ppm	HOLT 6A, With corrections
	(1)	AC Voltage Source	1 ppm resolution	FLUKE 5200A/5215A
Ω	(8)	Resistance Standards	Known within:	
		100Ω	30 ppm	ESI SR1 with corrections
		1 KΩ	30 ppm	ESI SR1 with corrections
		10 KΩ	30 ppm	ESI SR1 with corrections
		100 KΩ	30 ppm	ESI SR1 with corrections
		1 MΩ	30 ppm	ESI SR1 with corrections
		10 MΩ	30 ppm	ESI SR1 with corrections
OTHER	(1)	Momentary Switch, SPST	–	–
	(2)	1.5 volt cells w/screwtype binding posts	–	–
	(1)	Insulated Adjustment tool	–	JFD5284
	(1)	100Ω, 10 Kilohm, 1 Megohm 1/4 Watt 5% Carbon Resistors	5%	–
	(1)	1 μFD non polar capacitor	–	–

Table 5.2 - DC Source and DMM Accuracies

Range	10 Volt Source	Voltage Divider	Total Accuracy	24 hr. DMM Full Scale Accuracy	Times Better
10	10 ppm	–	10 ppm	100 ppm	10
1	10 ppm	1 ppm	11 ppm	100 ppm	9
100mV	10 ppm	1 ppm	11 ppm	100 ppm	9
100	10 ppm	1 ppm	11 ppm	100 ppm	9
1000	10 ppm	1 ppm	11 ppm	100 ppm	9

also as a reference for generating highly accurate .1, 1, 100, and 1000 volt levels. The 10 volt source used must satisfy the following requirements.

a. It must be traceable to the National Bureau of Standards;

b. It must have a total accuracy of ±10 ppm;

c. It must have a low output impedance.

5.2.3.2 A source filling these requirements is shown in Figure 5.1. This circuit consists of a null detector, 7-decade voltage divider, a DC voltage supply, and a bank of saturated standard cells. Two advantages of this particular hookup are that; (a) there is minimal loading of the standard cells and (b) stability, not accuracy, is the primary requirement of the DC voltage supply. The output of this circuit is set to a precise 10 volts by setting the voltage divider to the value of the standard cells. The DC voltage source is then adjusted to produce a null on the null detector. The accuracy of the 10 volt source is within ±10 ppm. The remainder of the DC sources can be generated by the circuits shown in Table 5.4 and 5.5. Each of these hookups use a calibrated 10 volt source having the characteristics of the one previously described.

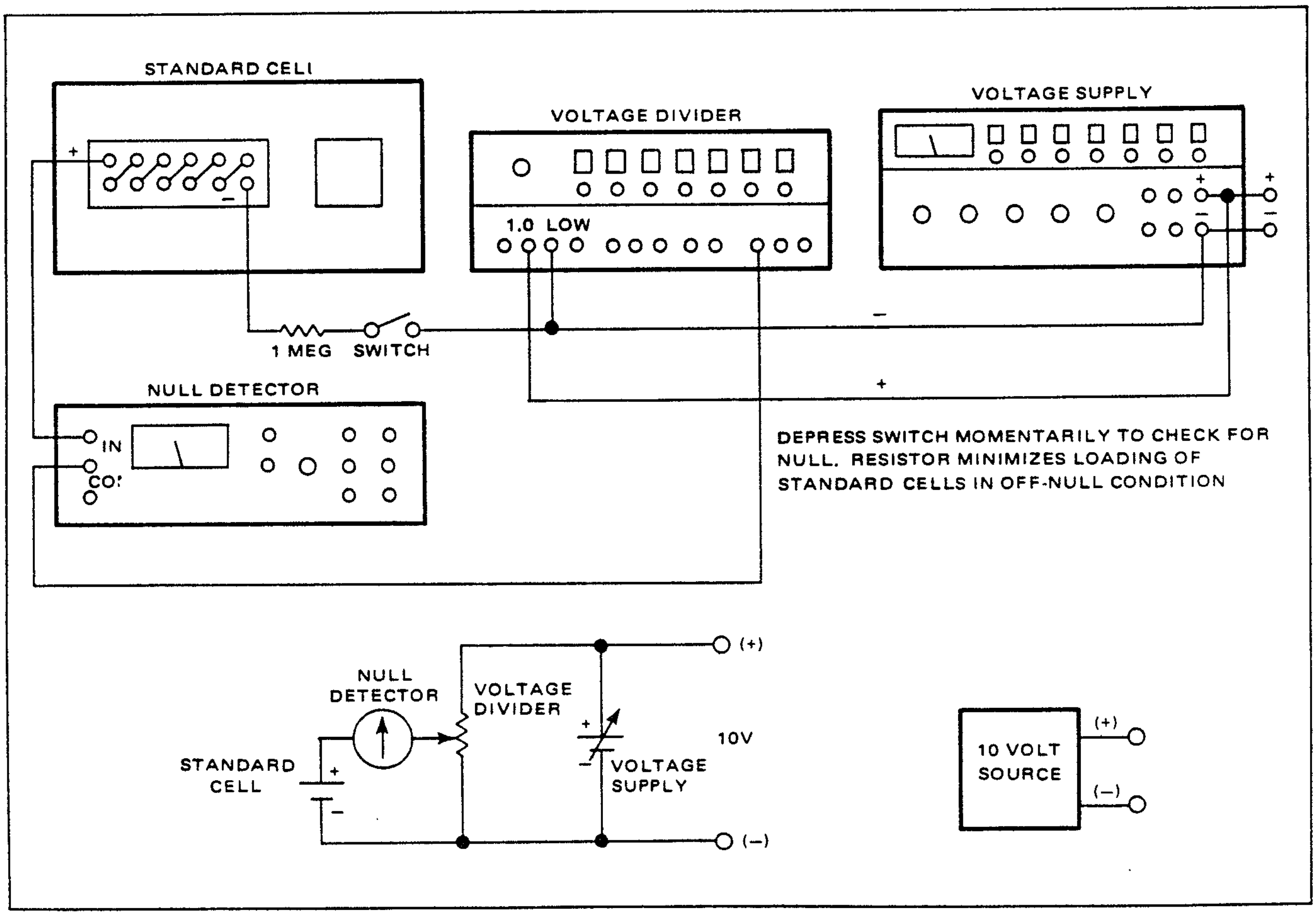


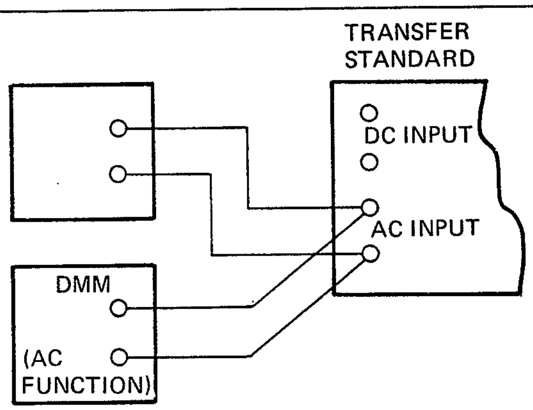
Figure 5.1 - 10 Volt Source

5.2.4 DC Accuracy.

5.2.4.1 The accuracy of the DC voltage sources is obtained by adding the various sources of error in each hookup; errors in this discussion are defined in parts per million (ppm). In Table 5.2 is shown the errors of each voltage source, the total accuracy of each hookup, the accuracy of the DMM, and the degree to which the sources exceed the required accuracy of the DMM (4 to 10 times better is the suggested accuracy ratio per MIL-M-38793).

5.2.5 AC Voltage Sources.

5.2.5.1 The generation of accurate AC signals for checking the AC converter ranges, requires the use of a thermal transfer standard and a precise DC standard as well as a stable AC source. Sufficient accuracy can be obtained by using a DC source and the DMM under test. The circuitry connections are shown in Figure 5.2. Information on the use of the transfer standard can be obtained from the operator's manual accompanying the standard. The DMM is used to set the DC source to the desired voltage and the thermal transfer is used to calibrate the output of the AC source. The calibrated AC source is used to check the DMM AC Converter. This procedure is repeated for each range.



The ac source is adjusted to produce a null on transfer standard. The ac source output is now calibrated and can be used as a precision source for the recalibration of the AC Converter.
NOTE: Because of the low input impedance of the transfer standard, the DMM input leads must be connected as close to the transfer standard input terminals as possible.

Figure 5.2 - AC Source

5.2.5.2 AC ACCURACY

5.2.5.2.1 The accuracy of the AC source is equal to the sum of the transfer-standard accuracy and the accuracy of DC source. The accuracy of the setup for each range and frequency used is provided in Table 5.3.

Table 5.3 - AC Source Accuracies

INPUT		ACCURACY		
AC Source				
Volts	Freq	Thermal Transfer Standard	DC Source	Total AC Source
1, 10, and 100 Volts	400 Hz	35 ppm	10 ppm	45 ppm
	50 kHz	50 ppm		60 ppm
500 Volts	40 kHz	50 ppm		60 ppm
1000 Volts	400 Hz	52 ppm		62 ppm

5.2.6 Test Procedures.

5.2.6.1 Allow two hours for warmup. Connect the instrument and the test equipment as shown in the figure supplied with each accuracy check. Select the controls and inputs as called out in the tables and monitor the instrument readout for the indicated values. Proceed with the tests described in Tables 5.4 through 5.9.

WARNING

The following procedures include the use of high voltage sources producing potentially lethal voltages. Avoid contact with high voltage terminals.

5.3 CALIBRATION.

5.3.1 This instrument was calibrated to published specifications in Racal-Dana test Labs prior to shipment. The procedures in this section are designed to maintain calibration and keep the instrument operating within specifications.

5.3.2 Required Equipment.

5.3.2.1 A list of equipment required for calibration is given in Table 5.1. The specific equipment types are given only as a guide. If substitutions are made, the substituted equipment must meet or exceed the specifications of the equipment listed.

5.3.3 DC & AC Voltage Sources.

5.3.3.1 See Sections 5.2.3, 5.2.4, and 5.2.5.

5.3.4 Calibration Principles.

5.3.4.1 Calibration procedure for the DMM utilizes microprocessor controlled adjustments. The calibration adjustments executed through the keyboard input or GPIB commands are the software method of setting correction factors.

5.3.4.2 The Non-Volatile Constants memory of the DMM enables the microprocessor to perform software calibrations. Inputs are applied to the DMM from the calibration standard and the reading is incremented or decremented via keyboard control or GPIB commands until the reading equals the input standard. During this process, the numeric constants for analog offset voltages and scale factor corrections are loaded into the Non-Volatile memory by the microprocessor (μP). These constants are then used by the μP to correct each DMM reading before display or readout to the GPIB.

5.3.4.3 In order to enter correction constants into the Non-Volatile memory, three conditions are required:

a. The correct input standard for the function and range selected is applied to the DMM.

b. The calibration switch (Cal-Sw) must remain depressed during the adjustment process.

c. A keyboard input or GPIB command is required to increment or decrement the reading to equal the input standard.

IMPORTANT REMINDER

KEYBOARD OR GPIB CALIBRATION COMMANDS ARE "NOT" EFFECTIVE UNLESS THE CAL-SW IS HELD IN THE DEPRESSED POSITION. NUMBERS ARE ENTERED INTO THE NON-VOLATILE MEMORY ONLY WHEN THE CAL-SW IS IN THE "DEPRESSED POSITION".

5.3.4.4 The Cal-Sw is a momentary contact switch accessible through an opening on the front panel (see Figure 3.1 No. 8 for location). The switch can be depressed by inserting an appropriate size screwdriver or similar tool through the opening.

5.3.4.5 The DMM Function, Range and Input Standard for each entry into the Non-Volatile memory is listed in Table 5.10. One offset correction factor is entered for each Function and a scale factor is entered for each Range. In the DC Function, scale factors are entered for both positive and negative inputs, additionally a scale factor correction constant is entered for the 4 1/2 digit mode.

Table 5.4 - DC Function Check (Low Ranges)

DVM		INPUT SIGNAL				
FUNCTION	RANGE	DC VOLTAGE STANDARD	VOLTAGE DIVIDER SETTING	NOMINAL READING	TOLERANCE (6 MO. SPEC.) 5-1/2 DIGIT MODE	NOTE
DC	.1V	10.00000	.01000	.100000	.099974 – .100026	23°C ± 5°C (After DIGITAL ZERO Command)
		10.00000	.02000	.200000	.199954 – .200046	
	1V	10.00000	.10000	1.00000	.99984 – 1.00016	
		10.00000	.20000	2.00000	1.99974 – 2.00026	

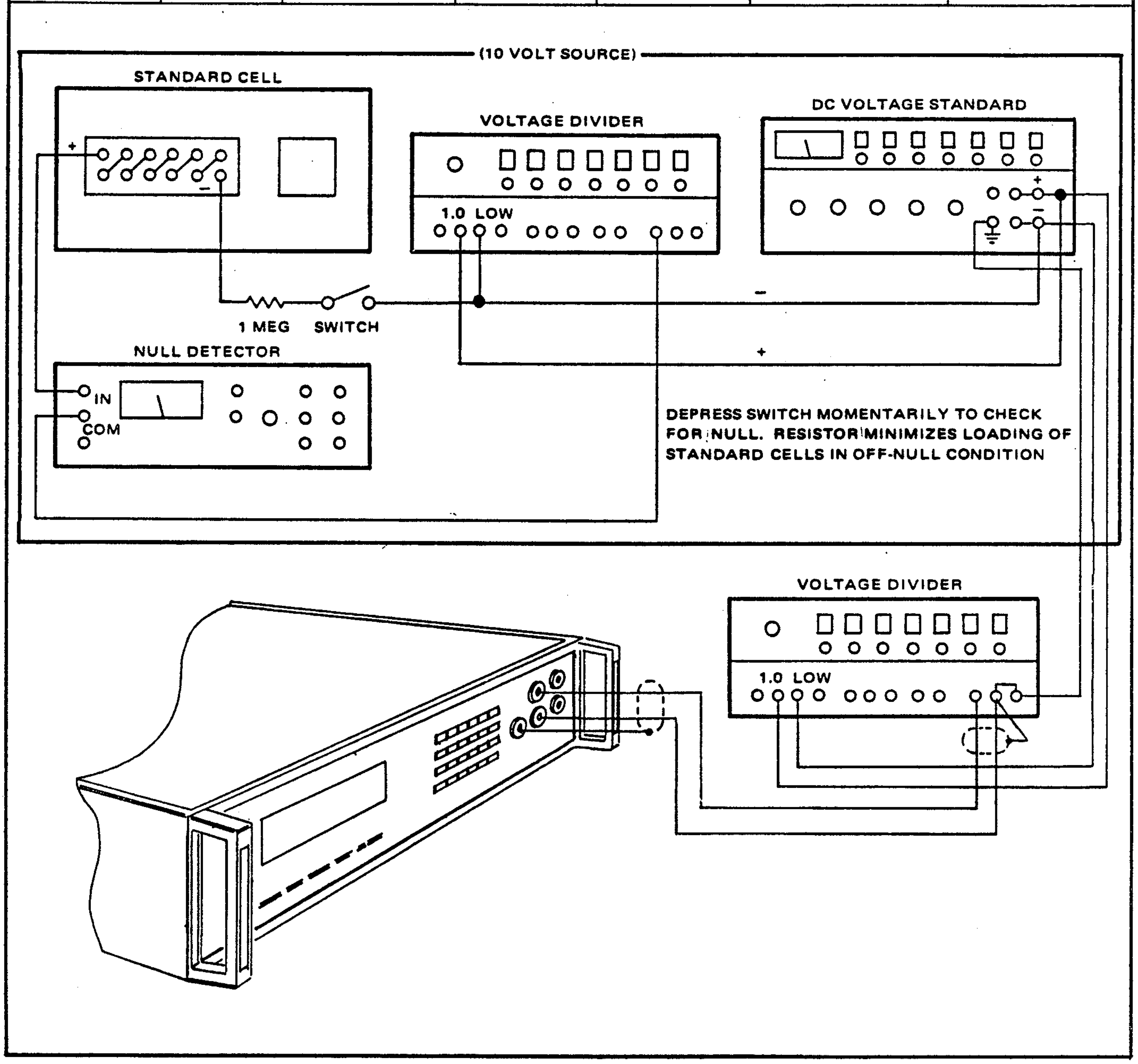


Table 5.5 - DC Function Check (High Ranges)

DVM		INPUT SIGNAL		NOMINAL READING	TOLERANCE (6 MO. SPEC.) 5-1/2 DIGIT MODE	NOTE
FUNCTION	RANGE	DC VOLTAGE STANDARD	VOLTAGE DIVIDER SETTING			
DC	10	10.0000V	1.0000	10.0000	9.9974 – 10.0026	23°C ± 5°C (After DIGITAL ZERO Command)
		20.0000V	.50000	20.0000	19.9954 – 20.0046	
	100	100.000V	.10000	100.000	99.974 – 100.026	
		200.000V	.05000	200.000	199.954 – 200.046	
	1000	1000.00V	.01000	1000.00	999.74 – 1000.26	

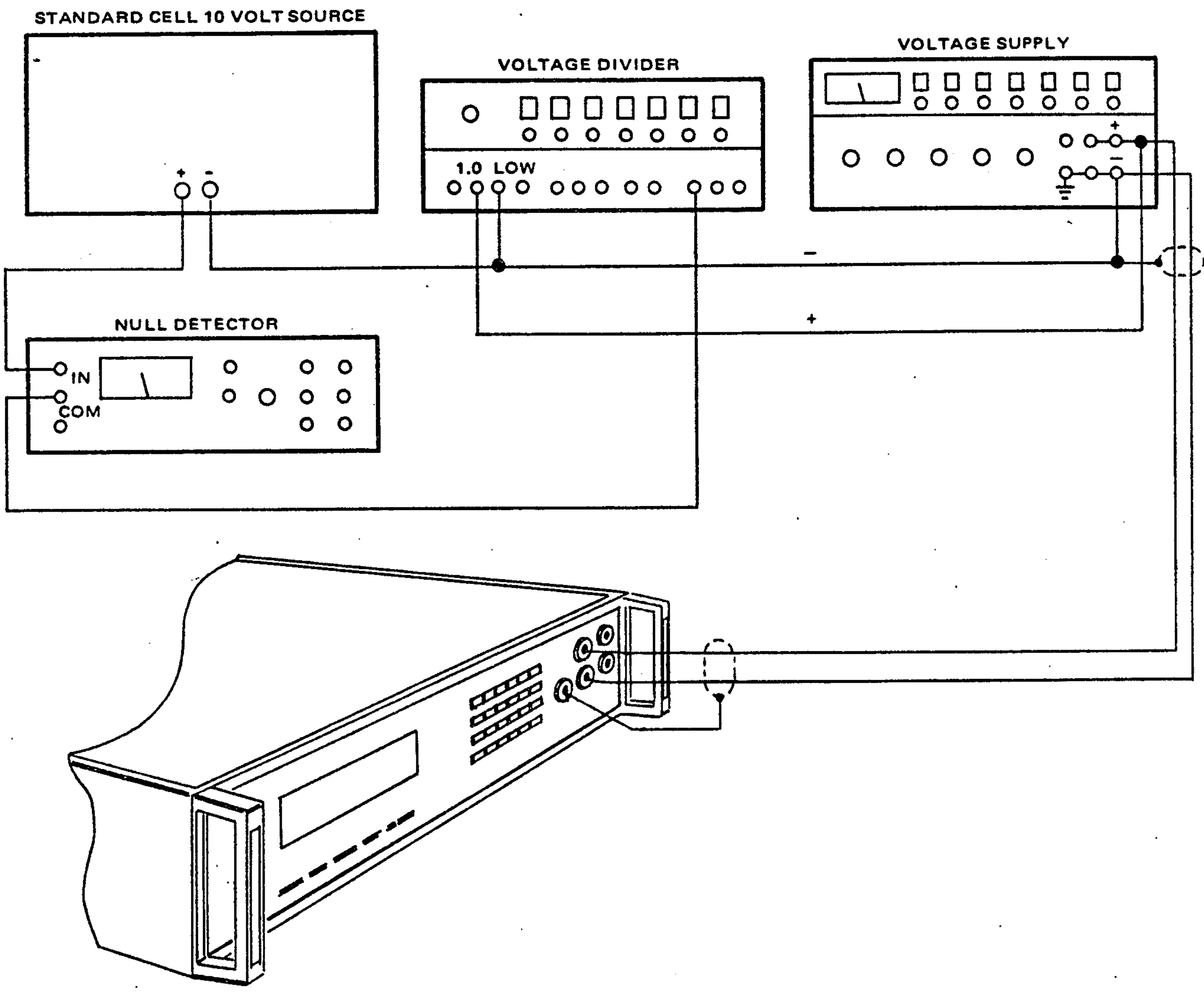
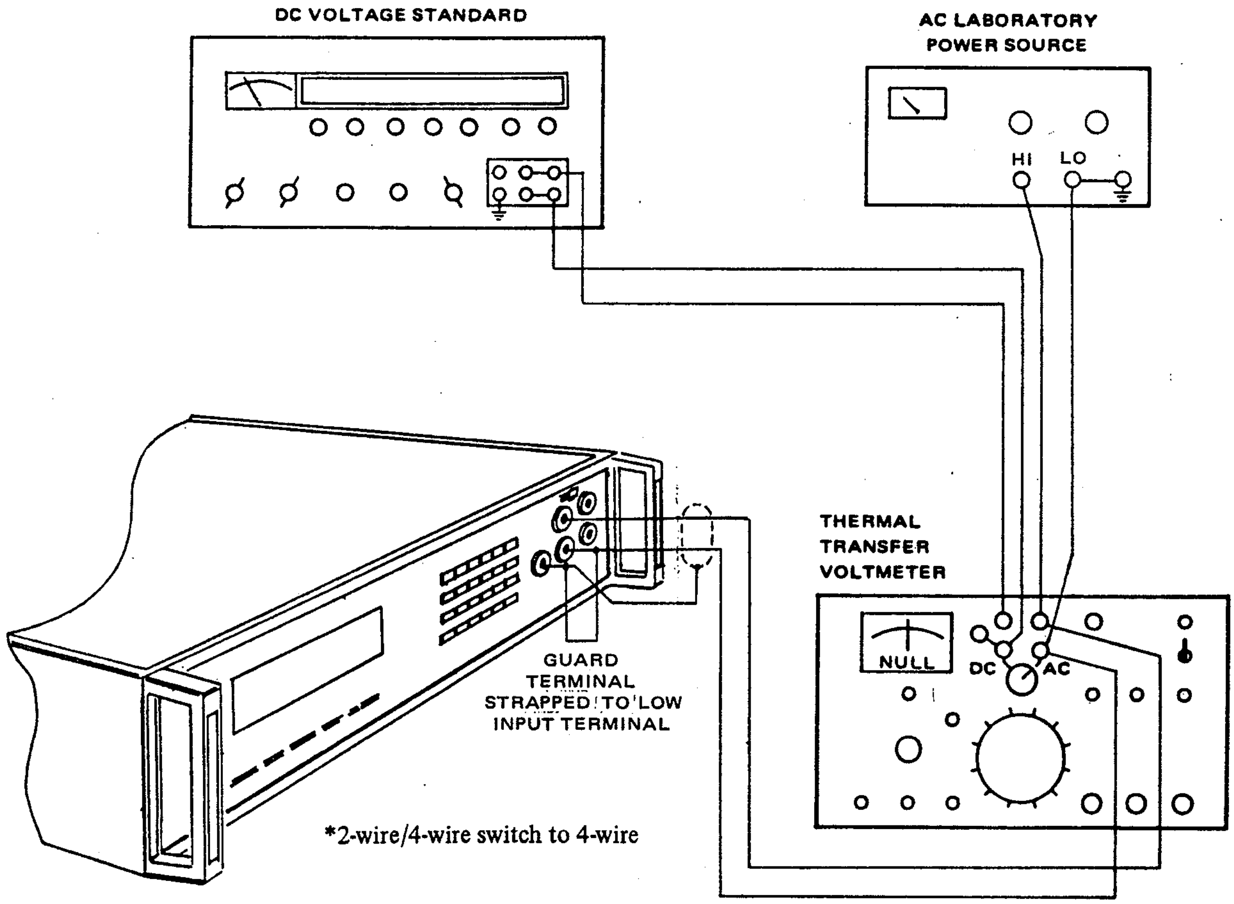


Table 5.6 - Averaging AC Converter Range Check Model 5005

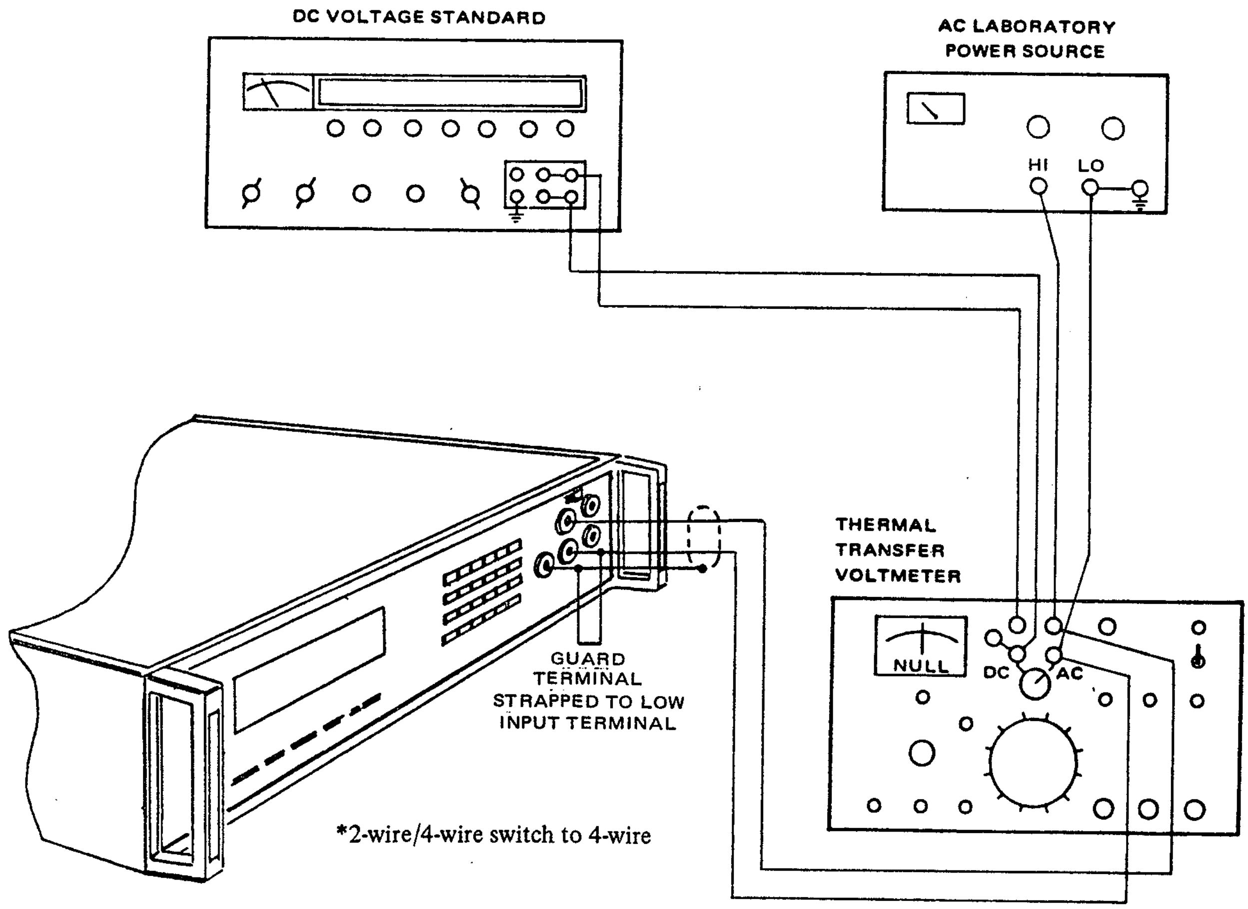
DVM		INPUT SIGNAL		NOMINAL READING (5-1/2 Digit Mode)	TOLERANCE	NOTE (6 Month Spec)
FUNCTION	RANGE	DC VOLTAGE STANDARD	AC			
AC	1	1.000000	1V @ 400 Hz	1.00000	.99880 – 1.00120	23°C ± 5°C (After Auto Cal) *
		1.000000	1V @ 50 kHz	1.00000	.99830 – 1.00170	
	10	10.00000	10V @ 400 Hz	10.0000	9.9880 – 10.0120	
		10.00000	10V @ 50 kHz	10.0000	9.9830 – 10.0170	
	100	100.0000	100V @ 400 Hz	100.000	99.880 – 100.120	
		100.0000	100V @ 50 kHz	100.000	99.830 – 100.170	
	1000	1000.000	1000V @ 400 Hz	1000.00	997.80 – 1002.20	
		500.000	500V @ 40 kHz	500.00	498.55 – 501.45	



*2-wire/4-wire switch to 4-wire

Table 5.7 - RMS AC Converter Range Check (Model 5006)

DVM		INPUT SIGNAL				
FUNCTION	RANGE	DC VOLTAGE STANDARD	AC	NOMINAL READING (5-1/2 Digit Mode)	TOLERANCE	NOTE (90 Day Spec) (AC Coupled)
AC	1	1.000000	1V @ 400 Hz	1.00000	.99840 – 1.00160	23°C ± 5°C (After Auto Cal) * Add ± 20 digits to spec if DC coupled mode is selected on AC Converter
		1.000000	1V @ 50 kHz	1.00000	.99800 – 1.00200	
	10	10.00000	10V @ 400 Hz	10.0000	9.9840 – 10.0160	
		10.00000	10V @ 50 kHz	10.0000	9.9800 – 10.0200	
	100	100.0000	100V @ 400 Hz	100.000	99.840 – 100.160	
		100.0000	100V @ 50 kHz	100.000	99.800 – 100.200	
	1000	1000.000	1000V @ 400 Hz	1000.00	997.40 – 1002.60	
		500.000	500V @ 40 kHz	500.00	498.00 – 502.00	



*2-wire/4-wire switch to 4-wire

Table 5.8 - K Ohms Function

DVM		INPUT SIGNAL		TOLERANCE* (6 MO. SPEC.) 5-1/2 DIGIT MODE	NOTE
FUNCTION	RANGE	NOMINAL STANDARD VALUE			
KΩ	.1KΩ	100Ω		± 110 digits	23°C ± 5°C
	1 KΩ	1 KΩ		± 110 digits	
	10 KΩ	10 KΩ		± 110 digits	
	100 KΩ	100 KΩ		± 110 digits	
	1000 KΩ	1 MΩ		± 110 digits	
	10000 KΩ	10 MΩ		± 110 digits	

*After DIGITAL ZERO Command.

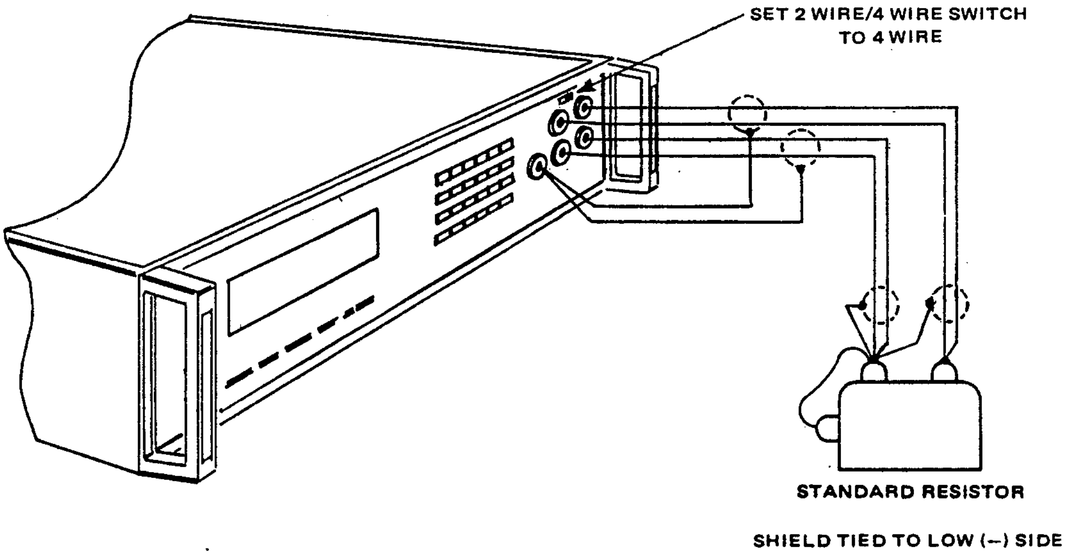


Table 5.9 - Normal Mode Noise Rejection (In DC Volts Function)

DVM		INPUT SIGNAL		NOMINAL READING	TOLERANCE	NOTE
FUNCTION	RANGE	DC	AC			
DC	10	0.5V	7.07V RMS 60 Hz*	00.5000	± 100 digits	

*50 Hz for 50 Hz Instruments.

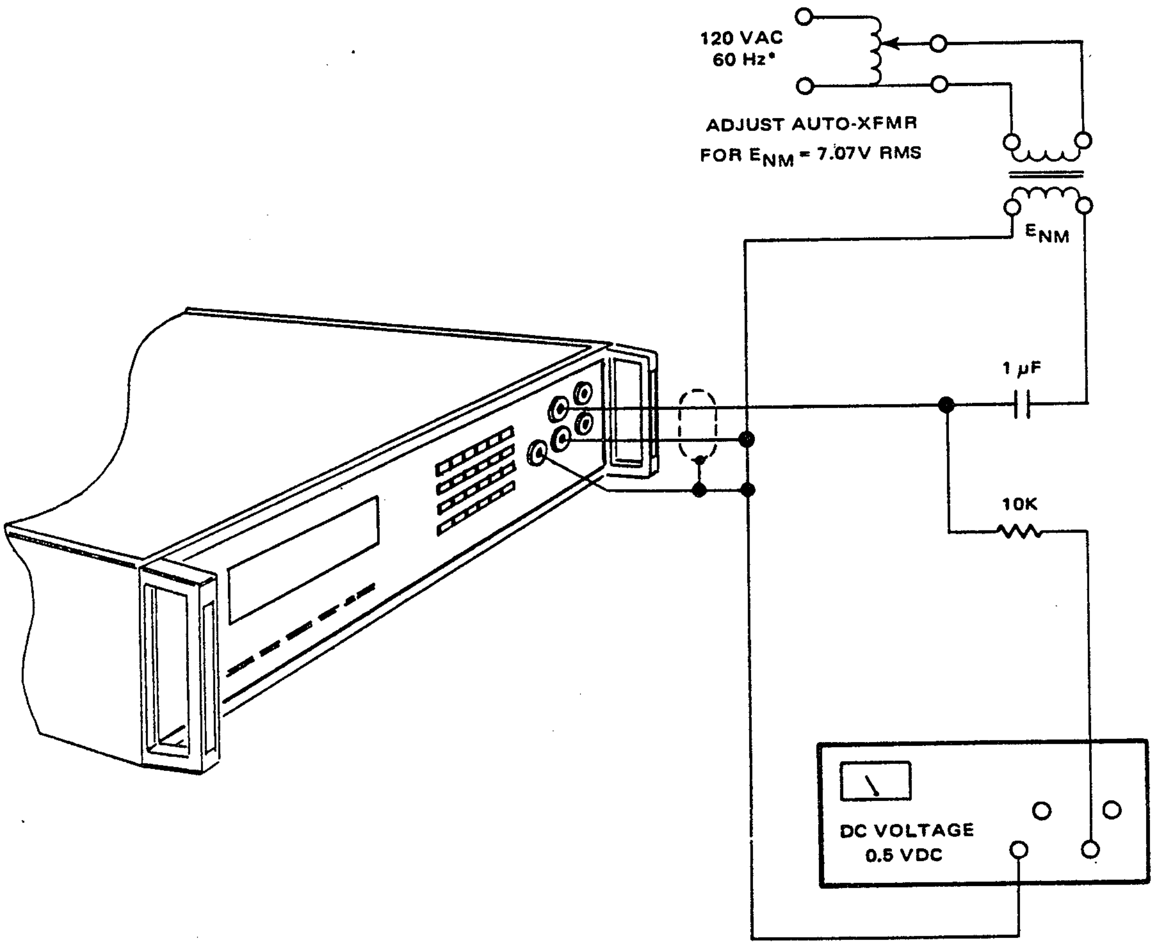
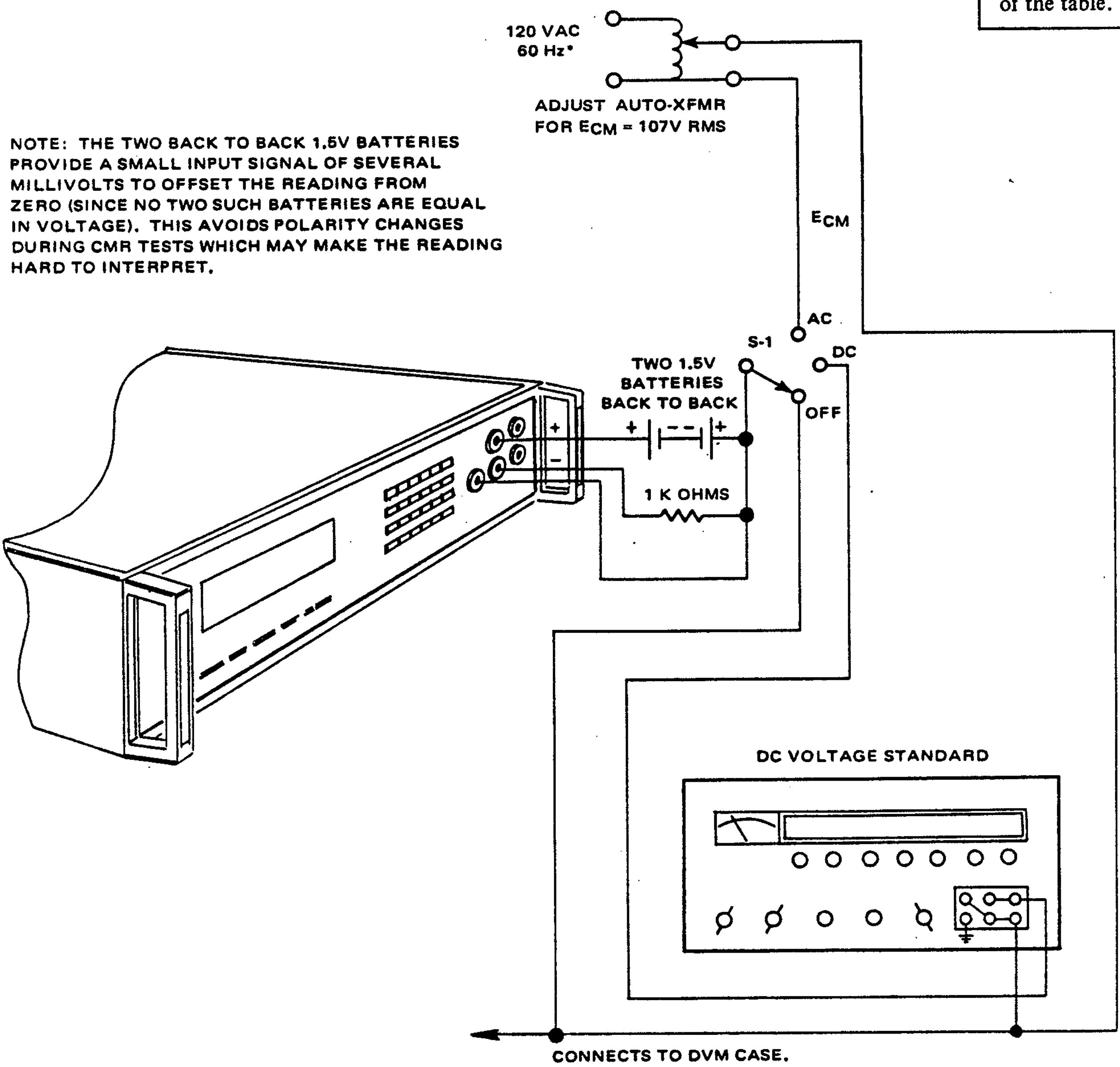


Table 5.10 - Common Mode Rejection (In DC Volts Function)

DVM		INPUT SIGNAL		NOMINAL READING See Note 1	TOLERANCE	NOTE
FUNCTION	RANGE	S1				
DCV	1V	Off				1) With switch S-1 in the off position, record the reading displayed on the DMM's readout in the "nominal reading" boxes of the table.
		DC	1000V		± 10 digits from nominal	
		AC	107V RMS 60 Hz*		30 digits peak-to-peak	

*50 Hz for 50 Hz Instruments.



5.3.4.6 MANUAL CALIBRATION

5.3.4.6.1 The DMM procedure to enter corrections using the keyboard command is as follows:

a. Offset Correction Factors: Zero volts or ohms are applied to the DMM.

b. Scale Factor Corrections: A full scale input is applied in each Function and Range.

c. Three input keys on the keyboard which perform the UP count, DOWN count, and NOMINAL functions are described below.

1. UP Key: Performed by depressing the RECALL key and referred to as RECALL/UP. This key increments the numbers in memory while the Cal-SW is held depressed.

2. DOWN Key: Performed by depressing the STORE key and referred to as STORE/DOWN. This key decrements the numbers in memory while the Cal-SW is held depressed.

3. NOMINAL Key: Performed by depressing the RESET key and referred to as RESET/NOMINAL. This key initializes the numbers in memory while the Cal-SW is held depressed, as explained in the next paragraph.

Table 5.11 - Non-Volatile Memory Constants

Memory Constant	Calibration Conditions		
	Function	Range	Input
DC Offset	DC	0.1 V	Zero
.1V Pos. Scale Factor	DC	0.1 V	+ 0.1 V DC
.1V Neg. Scale Factor	DC	0.1 V	−0.1 V DC
1V Pos. Scale Factor	DC	1V	+1VDC
1V Neg. Scale Factor	DC	1V	−1VDC
10V Pos. Scale Factor	DC	10V	+10VDC
10V Neg. Scale Factor	DC	10V	−10VDC
100V Pos. Scale Factor	DC	100V	+100VDC
100V Neg. Scale Factor	DC	100V	−100VDC
1KV Pos. Scale Factor	DC	1KV	+1KVDC
1KV Neg. Scale Factor	DC	1KV	−1KVDC
4 1/2 Digit Scale Factor	DC	1V	±2VDC
AC Offset	AC	1KV	Zero
1V Scale Factor	AC	1V	1V RMS, 400 Hz
10V Scale Factor	AC	10V	10V RMS, 400 Hz
100V Scale Factor	AC	100V	100V RMS, 400 Hz
1KV Scale Factor	AC	1KV	1 KV, 400 Hz
Ohms Offset	KΩ	100K	Zero
.1KΩ Scale Factor	KΩ	0.1 K	100Ω
1KΩ Scale Factor	KΩ	1K	1KΩ
10KΩ Scale Factor	KΩ	10K	10KΩ
100KΩ Scale Factor	KΩ	100K	100KΩ
1000KΩ Scale Factor	KΩ	1000K	1MΩ
10,000KΩ Scale Factor	KΩ	10,000K	10MΩ

5.3.4.6.2 The RESET/NOMINAL key is used to initialize the numbers in Non-Volatile memory. When this key is depressed and released, either a ZERO is entered into the Non-Volatile memory as an offset correction factor, provided the DMM input is less than 40% of full scale, or a ONE is entered into the Non-Volatile memory as a scale factor, provided the DMM input is greater than 40% of full scale.

5.3.4.6.3 The STORE/DOWN key decrements the numbers in the Non-Volatile memory. This action is described as follows:

a. When entering an offset correction factor, this key changes the reading in a "Negative going" direction. For example, if the DMM reading is .00023 for zero input in the DC function, each time the STORE/DOWN key is depressed and released, the reading will decrease one digit. Upon reaching .00000, calibration of the DC offset correction factors is complete. Further depression of this key will cause the reading to increase with a negative polarity indication.

b. When entering scale factors, each depression of the STORE/DOWN key will decrease the displayed reading one digit when a Full Scale Input is applied.

c. When the decrements required for corrections are numerous, holding the STORE/DOWN key depressed longer than two seconds approximately, will decrement the readings as a faster rate as long as the key remains depressed.

5.3.4.6.4 The RECALL/UP key increments the numbers in the Non-Volatile memory. This action is described as follows:

a. When entering an offset correction factor, this key changes the reading in a "Positive going" direction. For example, if the DMM reading is −.00023 for zero input in the DC Function, each time the RECALL/UP key is depressed and released, the reading will decrease one digit. Upon reaching .00000, calibration of the DC offset correction factor is complete. Further depression of this key will cause the reading to increase with a positive polarity indication.

b. When entering scale factors, each depression of the RECALL/UP key will increase the display reading one digit as a Full Scale input is applied.

c. When the increments required for corrections are numerous, holding the RECALL/UP key depressed longer than two seconds approximately, will increment the readings at a faster rate as long as the key remains depressed.

5.3.4.6.5 In situations where the input standard and the initial reading differ by several hundred digits, the difference can be reduced at the fastest rate by switching to the 4 1/2 digit mode (depress and release RESOL key). In the 4 1/2 digit mode, each depression of the RECALL/UP or STORE/DOWN key changes the reading one digit, which is 10 digits on the 5 1/2 digit mode. Holding either key depressed for fast increment or decrement operation also changes the reading in 10 digit increments. Once the reading has been reduced to within a few digits of the input standard in the 4 1/2 digit mode, switch back into the 5 1/2 digit operation to complete the calibration.

5.3.4.6.6 When using the 4 1/2 digit mode to change the reading rapidly, the DMM "must be in a fixed range" (AUTO ranging disabled and AUTO annunciator OFF). When this precaution is not taken, the 4 1/2 digit Scale Factor will be modified instead of the desired Non-Volatile memory constant.

5.3.4.6.7 If the 4 1/2 digit Scale Factor is inadvertently modified, the 4 1/2 and 5 1/2 digit readings will differ. To re-initialize the 4 1/2 digit Scale Factor, the following procedure is presented.

a. Select the DC Function any Range, 4 1/2 digit mode, Auto-ranging (Auto-annunciator ON).

b. Apply a full scale input to the DMM for the Range selected in (a.).

c. Depress and hold the calibration switch.

d. Depress and release the RESET/NOMINAL key.

e. Release the calibration switch.

WARNING

These instructions are for use by qualified personnel only. To avoid electric shock, do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so.

5.3.4.7 GPIB CALIBRATION

5.3.4.7.1 When calibration is performed via the GPIB, it is convenient to short the Cal-Sw terminals with a temporary jumper. The Cal-Sw drawing shown in Figure 5.3 indicates the location of the jumper.

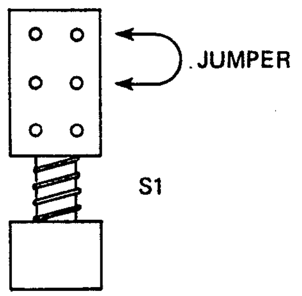


Figure 5.3 - Cal-Switch, Top View

IMPORTANT

Connect the jumper after power is applied to the DMM and disconnect the jumper before power is removed. If this instruction is not followed, the contents of the Non-Volatile memory will be destroyed and "Error 4" will be displayed the next time power is applied to the DMM.

5.3.4.7.2. GPIB commands K3 through K5 affect the Offset constant for the Function which is presently programmed. Each transmission of the K3 or K5 command to the DMM is equivalent to applying a low-level input (Low level is less than 40% and high-level is greater than 40% of Full Scale.), and momentarily pressing the STORE/DOWN or RECALL/UP keys on the DMM front panel. Transmitting the K4 command is equivalent to the keyboard procedure for initializing offset constants, with the exception that the input signal need not be less than 40% of full scale when initializing offset constants over the bus.

5.3.4.7.3 GPIB commands K6 through K8 affect the Scale constants for the range which is presently programmed. Each transmission of the K6 or K8 command to the DMM is equivalent to applying a high level input and momentarily pressing the STORE/DOWN or RECALL/UP keys on the DMM front panel.

5.3.4.7.4 Transmitting the K7 command has the same effect as initializing scale constants from the keyboard. To initialize a scale factor over the GPIB, the following procedure is provided:

a. Apply a high-level input signal.

b. Complete at least one reading on the presently programmed function/range.

c. Transmit the K7 command to the DMM.

> **NOTE**
>
> The K4 and K7 commands should not be required unless the contents of the non-volatile are destroyed.

5.3.5 Calibration Procedure.

> **NOTE**
>
> Initialize the non-volatile memory, as described in section 5.3.6, with "reasonable" Cal factors to prevent improper function of the Cal memory.
>
> If repairs were completed recently, refer to section 5.3.6 for instructions.

5.3.5.1 INPUT BIAS CURRENT NULL (R53).

a. Connect the Decade Resistance Box across the INPUT terminals. Select DC Function, .1V Range and FILTER.

b. Allow instrument at least one hour warmup with covers in place.

c. Switch Decade Resistance Box between 0 and 1 Megohm. If display changes more than ± 50 digits as Decade box is switched, proceed to steps (d.) and (e.).

> **WARNING**
>
> Removal of covers exposes potentially lethal voltages. Avoid contact with internal electrical connections while unit is connected to AC Power source.

d. Remove top cover for access to R53, but keep cover in place when not adjusting R53.

e. Adjust R53 until display changes less than ± 50 digits as Decade box is switched between 0 and 1 megohm. See Figure 5.8 for R53 location.

5.3.5.2 MODEL 5005 (AVERAGING AC PRE-CALIBRATION PROCEDURE

5.3.5.2.1 Model 5005 pre-calibration procedure reference drawings are shown in Figures 5.4 and 5.5. The procedures are described in the following paragraphs:

a) Set the DMM to AC and the 1V range.

b) Apply 100 mV at 400 Hz from the AC calibrator to the HI-LO Input terminals.

c) Adjust R19 on the AC-PCB (section 2-a) for minimum (most negative readout).

d) Refer to Figure 5.4 - a functional diagram, and Figure 5.5 - the component location of the AC converter.

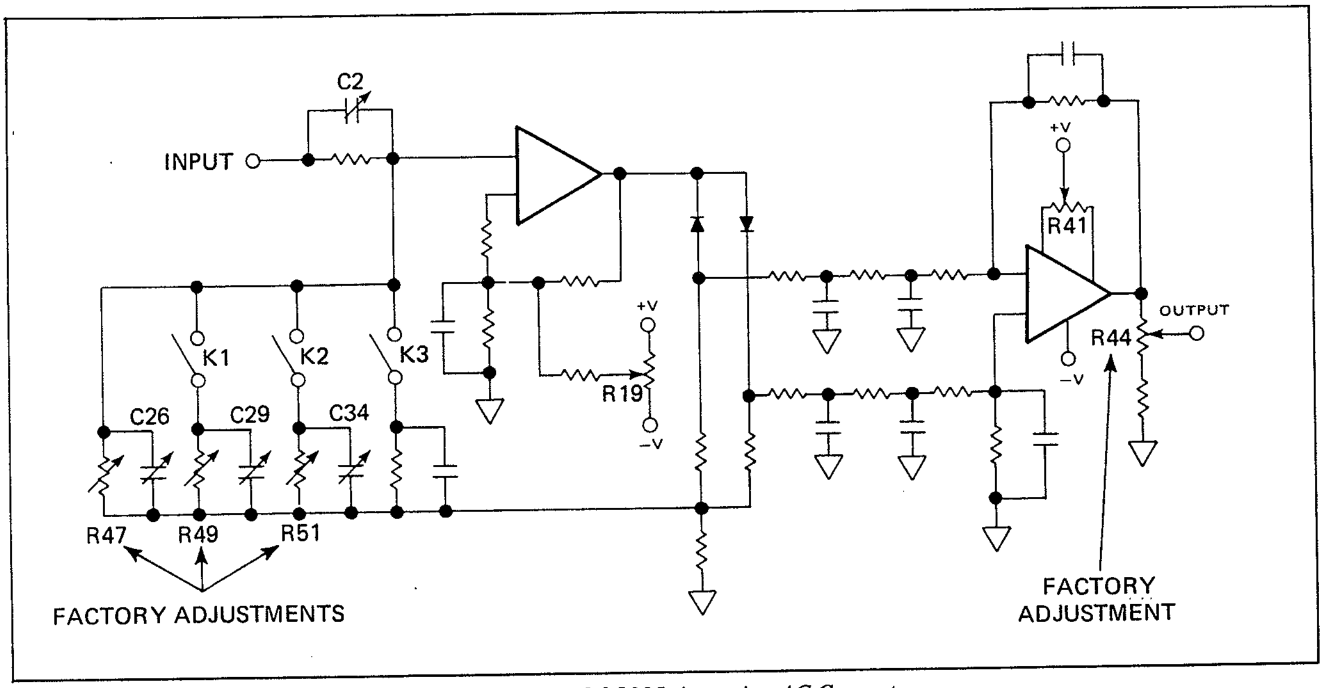


Figure 5.4 - Model 5005 Averaging AC Converter

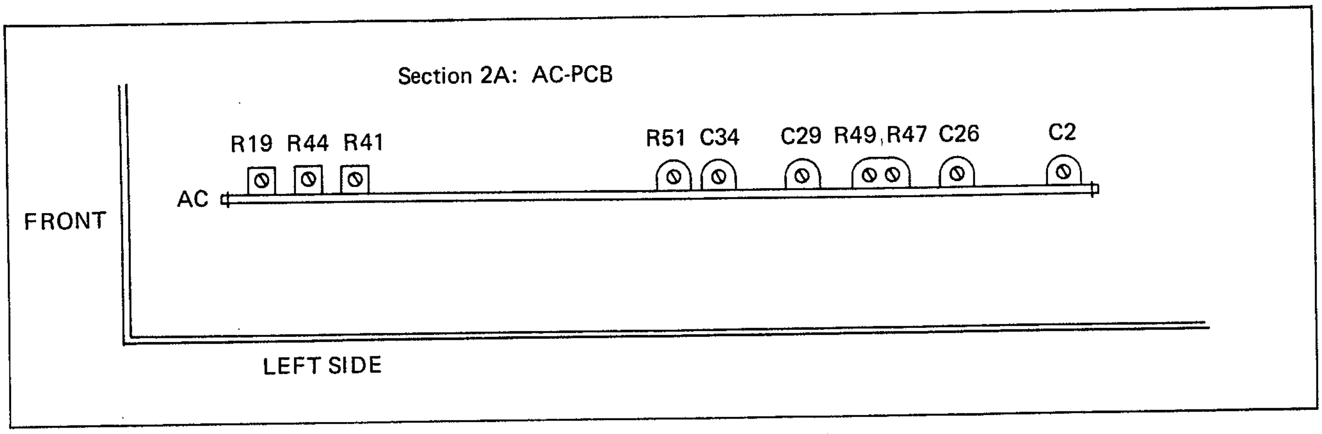


Figure 5.5 - Model 5005 Calibration Points

5.3.5.3 MODEL 5006 (RMS) AC PRE-CAL PROCEDURE

5.3.5.3.1 Model 5006 AC Pre-Cal procedure reference drawings are shown in Figures 5.6 and 5.7. The calibration procedures are described in the following instructions.

5.3.5.3.2 Select AC 1V range and short the DMM's input terminals together. Connect a micro voltmeter between TP6 (+) and TP1 (–) on the motherboard. If the microvoltmeter reading is greater than 0 ± 300 microvolts, perform the steps of the pre-cal adjustment procedure listed below.

a) Set DVM power switch to off. Extract converter and remote environmental shield. Set S1 and S2 to DC (toward center of board), replace converter and set power switch to on. Select AC and 1 volt range on DVM front panel. Allow 10 minutes for temperature to stabilize.

b) Connect jumper across DVM input terminals. Connect the microvoltmeter to TP2 (+) and TP5 (–). Adjust R17 for a microvoltmeter reading of 0 ± 30 μV. Remove + microvoltmeter lead from TP2. Turn R38 fully clockwise.

c) Connect microvoltmeter + lead to TP4.. Adjust R41 for a microvoltmeter reading of +20 ± 10 μV.

d) Connect + microvoltmeter lead to TP1. Adjust R28 for a microvoltmeter reading of 0 ± 30 μV. Remove microvoltmeter + lead from TP1.

e) Connect + microvoltmeter lead to TP3. Adjust R25 for 0 ± 30 mV. Remove + microvoltmeter lead from TP3.

f) Connect + microvoltmeter lead to TP4. Adjust R38 counterclockwise until the voltage at TP4 reads 0 + 5 μV. Remove microvoltmeter leads and remove jumper across DVM input.

g) Apply –1.00000V DC and note DVM display.

h) Reverse polarity of input to + 1.00000V DC and adjust R33 to obtain approximately the same DVM display as obtained in step g. Repeat steps g and h until the two readings are within .01% of each other. Remove DC supply from DVM input.

j) Reverse polarity of input to –0.100000 and verify DVM display is within + 5 digits of the reading obtained in step i. If not, use R25 to balance the readings. Select FILTER.

k) Set power switch on DVM to off, extract converter, set S1 and S2 to AC to their original position. Replace environmental shield on converter and replace converter in DVM. Reapply power and allow 10 minutes for temperature to stabilize.

5.3.5.4 "DIGITAL" CALIBRATION.

a. Verify that all shields and covers are installed.

b. Short the INPUT terminals and GUARD terminal together.

c. Allow at least 2 hours warmup with covers installed before proceeding.

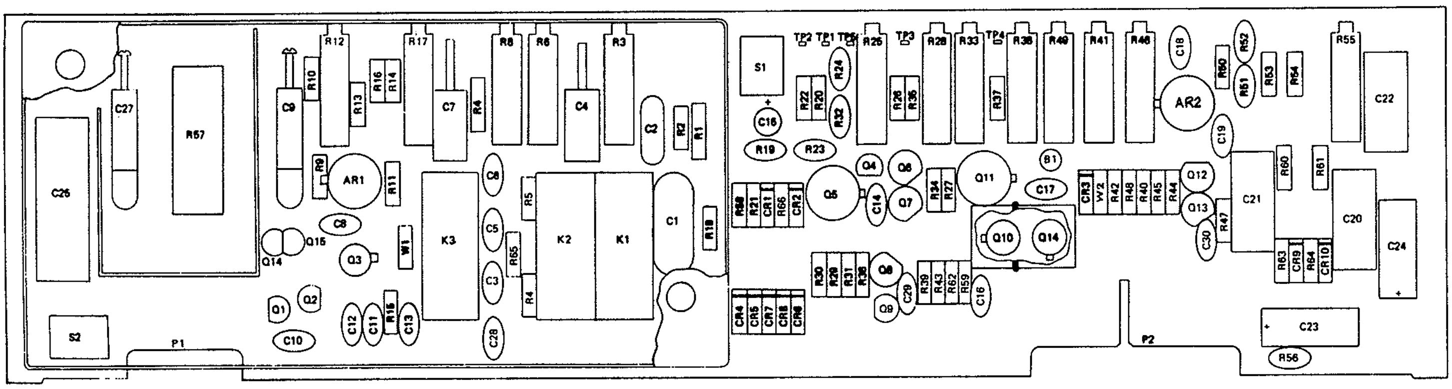


Figure 5.6 - RMS - PCB Assembly

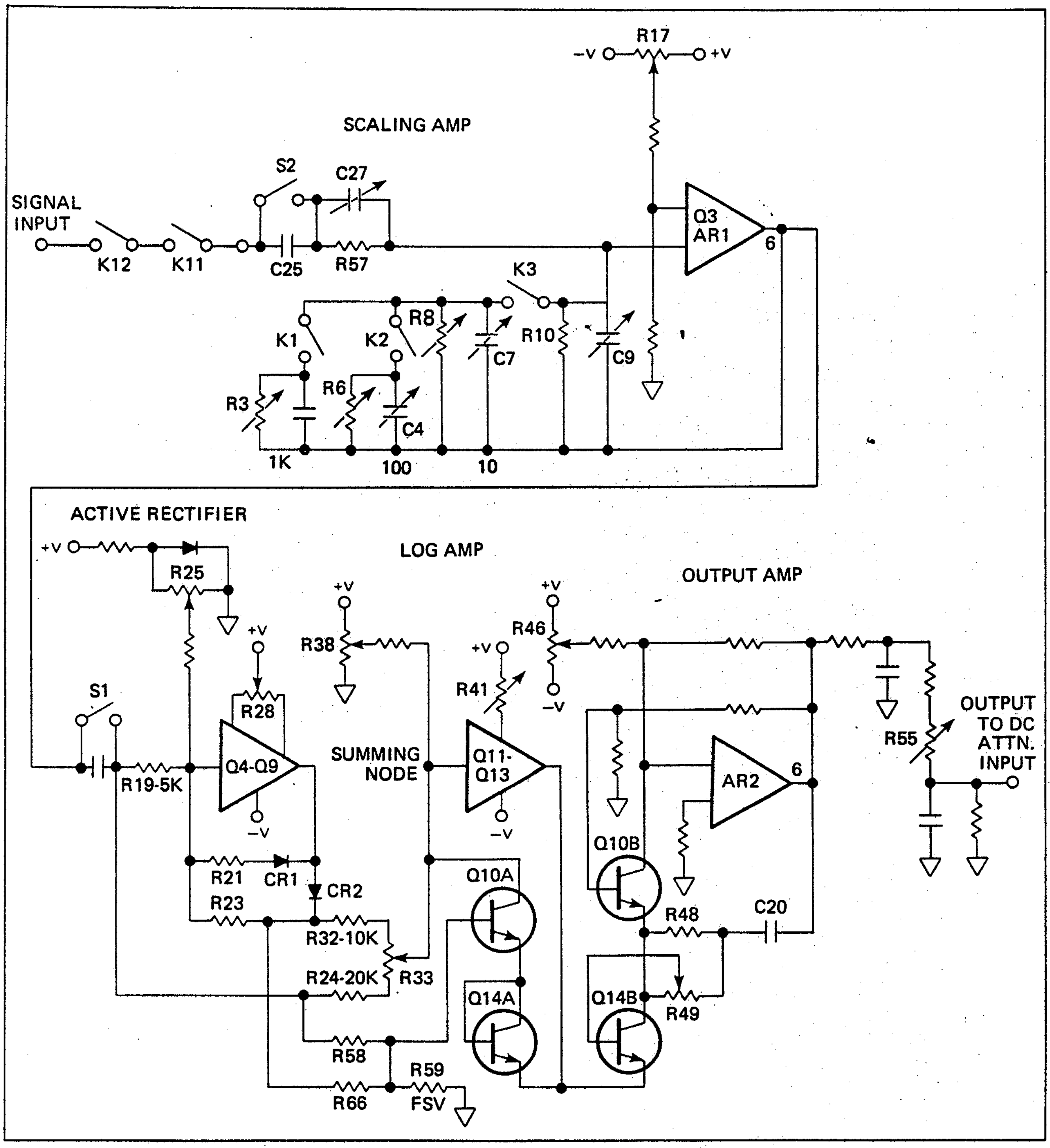


Figure 5.7 - Calibration Points

Table 5.12 - Calibration Points for Entry of Final Values Into Non-Volatile Memory

Function	Range	Input Standard	Input Connections	Notes
DC	.1V	0.00000 VDC	Table 5.4	Note 1 - See paragraph 5.3.5.5 to calibrate 4 1/2 Digit mode.
	.1V	+0.1 VDC		
	.1V	−0.1 VDC		
	1V	+1.0 VDC		
	1V	−1.0 VDC		
	1V	(Note 1)		
	10V	+10.0 VDC	Table 5.5	Note 2 - The value of the Resistance Standard must be known to within the tolerance indicated in Table 5.1.
	10V	−10.0 VDC		
	100V	+100.0 VDC		
	100V	−100.0 VDC		
	1KV	+1000.0 VDC		Note 3 - Range, Input Standard and procedure varies:
	1KV	−1000.0 VDC		
AC	See Note 3	See Note 3	Table 5.6	5005: Range: 1KV Input Standard: 0.0 VRMS
	1V	1.0V RMS, 400Hz		5006: Apply 0.100VAC at 400Hz and calibrate using procedure in sections 5.3.5.6f thru 5.3.5.6j. Perform next calibration point (1.0VRMS) using same procedure. Repeat 0.1 VRMS and 1.0VRMS calibrations until both are within specifications.
	10V	10.0V RMS, 400Hz		
	100V	100.0V RMS, 400Hz		
	1KV	1000.0V RMS, 400Hz		
KΩ	100KΩ	0.0Ω	Table 5.7	
	.1KΩ	100.0Ω	Note 2	
	1KΩ	1.0KΩ	Note 2	
	10KΩ	10.0KΩ	Note 2	
	100KΩ	100.0KΩ	Note 2	
	1000KΩ	1.0MΩ	Note 2	
	10,000KΩ	10.0MΩ	Note 2	

d. Select DC Function. Hold the .1V Range key depressed until "CAL 0" appears on the display, then release the Key.

e. Depress and hold the Calibration Switch.

f. Depress and release the RESET/NOMINAL Key.

g. Disable the Auto-range function by depressing the .1V Range Key. The AUTO annunciator will be OFF when disabled.

h. Refer to Table 5.12 for the Function, Range and Input for each calibration point. Verify that the AUTO annunciator remains OFF at each calibration point unless otherwise instructed.

5.3.5.5 5 1/2 DIGIT MODE CALIBRATION.

a. Connect the DMM to the Input Standard as specified for the first calibration point in Table 5.12. Set the K-V Divider to .009999X. Apply 0.00000 VDC to the DMM by shorting the input of the K-V Divider.

b. Depress and hold the Calibration Switch.

c. If the reading is not zero (4 digits p-p noise allowed), proceed to step (d); if equal to zero, release the Calibration Switch and proceed to step (f).

d. Increment or decrement the reading with the STORE/DOWN or RECALL/UP keys or GPIB command until the reading is zero.

e. Release the Calibration Switch.

f. Connect the DMM to the Input Standard as specified for the next calibration point in Table 5.12.

g. If the DMM reading is not equal to the Input Standard, proceed to step (h); if equal to the Standard, release the Calibration Switch and proceed to step (k.).

h. Depress and hold the Calibration Switch.

i. Increment or decrement the reading with the STORE/DOWN or RECALL/UP keys (or GPIB Command) until the reading is equal to the Input Standard.

j. Release the Calibration Switch.

k. Repeat steps (f.) thru (j.) for each calibration point in Table 5.12, except the 4 1/2 Digit Mode Scale Factor. At that step, see 5.3.5.5. Calibration is completed.

5.3.5.6 4 1/2 DIGIT MODE SCALE FACTOR CALIBRATION.

a. Switch to the 4 1/2 Digit Mode (depress RESOL Key) and Auto-ranging (depress AUTO Key - verify that AUTO annunciator is ON).

b. Apply +2.0000 VDC and note reading.

c. Apply −2.0000 VDC and note reading.

d. Depress and hold the Calibration Switch.

e. If the opposite polarity readings in (b) and (c) above are equal in magnitude, but not equal to 2.0000, increment or decrement either polarity reading with the STORE/DOWN or RECALL/UP Keys (or GPIB Command) until the readings are 2.0000 + 1 digit.

f. If the opposite polarity readings are not equal in magnitude, increment or decrement either polarity reading until the readings are within ±3 digits of 2.0000.

g. Release Calibration Switch.

5.3.5.7 AVERAGING AC FREQUENCY RESPONSE CALIBRATION–MODEL 5005

5.3.5.7.1 Perform the following instructions when frequency response calibration is required;

a) Connect the AC source to the DMM input terminals

b) Apply the inputs listed in the chart below.

c) Adjust the trimmers listed under "adjust" for the readout indicated. The trimmer locations are shown in Figure 5.5.

Range	INPUT		Adjust	Readout
	AC Voltage	Freq		
1000	250V	80kHz	C2	250.00
1	1V	100kHz	C26	1.00000
10	10V	100kHz	C29	10.0000
100	100V	100kHz	C34	100.000

5.3.5.8 RMS AC FREQUENCE RESPONSE CALIBRATION MODEL 5006

5.2.5.8.1 Perform the following instructions when frequency response calibration is required:

a) Connect the AC source to the DMM input terminals.

b) Apply the inputs listed in the chart below.

c) Adjust the trimmers listed under "adjust" for the readout indicated. The trimmer locations are shown in Figure 5.7.

Range	INPUT		Adjust	Readout
	AC Voltage	Freq		
1000V	500.00	40 kHz	C27*	500.000
1V	1.0000	50 kHz	C9*	1.00000
10V	10.000	50 kHz	C7*	10.0000
100V	100.00	50 kHz	C4*	100.000

*Use an insulated screwdriver when adjusting the capacitors. High voltage present on C27.

5.3.6 Adjustments After Repairs.

5.3.6.1 If major repairs are performed on the Isolator, AC Converter or Ohms Amplifier, offset and bias adjustments associated with these circuits may need adjustment. Also, if repair work is performed in the vicinity of the non-volatile memory, or battery power is interrupted, the contents of the non-volatile memory may be invalidated. This is indicated by the presence of the message "Error 4" shortly after power-up.

5.3.6.2 ISOLATOR ADJUSTMENT.

a. Input Bias Current Null (R53) - See paragraph 5.3.5.2.

5.3.6.3 INITIALIZING NON-VOLATILE MEMORY.

a. Refer to Table 5.13 for the Function, Range and Input for each Non-Volatile memory calibration point.

Table 5.13 - Inputs for Initializing Non-Volatile Memory

Function	Range	Input Standard (Note 1)
DC	.1V	0.0 VDC
	.1V	+0.1 VDC
	.1V	+0.1 VDC (Note 2)
	.1V	−0.1 VDC
	1V	+1.0 VDC
	1V	−1.0 VDC
	10V	+10 VDC
	10V	−10 VDC
	100V	+100 VDC
	100V	−100 VDC
	1KV	+1000 VDC
	1KV	−1000 VDC
AC	1V	0.0V RMS
	1V	1V RMS, 400 Hz
	10V	10V RMS, 400 Hz
	100V	100V RMS, 400 Hz
	1KV	1000V RMS, 400 Hz
KΩ	100KΩ	0.0Ω (Note 3)
	.1KΩ	100Ω (Note 3)
	1KΩ	1KΩ (Note 3)
	10KΩ	10KΩ (Note 3)
	100KΩ	100KΩ (Note 3)
	1000KΩ	1MΩ (Note 3)
	10,000KΩ	10MΩ (Note 3)

Note 1 - Unless otherwise noted, ± 10% accuracy is adequate.
Note 2 - Select 4 1/2 Digit mode (RESOL Key) and auto-ranging (AUTO Key) for this calibration only. Return to 5 1/2 Digit mode (RESOL Key), fixed range before continuing to the next step.
Note 3 - Either 2-wire or 4-wire connections are satisfactory.

b. At each point in the Table, set the DMM to the indicated Function and Range, and apply the specified input.

c. Depress and hold the Calibration switch.

d. While the Calibration Switch is held depressed, press and release the RESET/NOMINAL Key.

e. Release the Calibration Switch.

5.4 TROUBLESHOOTING.

5.4.1 General.

5.4.1.1 To troubleshoot the DMM and track-down malfunctions it is necessary to be familar with its normal operation. This manual is an important service tool, hence reading the complete manual is recommended.

5.4.1.2 A complete set of schematics for the DMM is contained in Section 6, which includes the parts list and parts lay-out. The components, IC's and logic symbols used in the schematic diagrams are identical to those found in most manufacturers data sheets. Whenever a designator appears which is unique to Racal-Dana, the description follows immediately.

5.4.1.3 The drawing interconnects and continuations to other sheets are indicated in the following manner:

a. Plugs and Jacks: "P" indicates the plug or movable section of the connector and J the jack or stationary connector. P or J with the numbers from 1 to 99 are used on the main PCB or motherboard locations, whereas P or J 100 series are on the front panel location and P or J 200 series represents the rear panel location. The E terminals are used for direct connection to the main PC board.

b. The drawing or schematic connection from one sheet to the next utilize the road-map grid system, with numbers along the horizontal edge and letters along the vertical edge of the drawing. A line terminating with a connection reference of 2B4 would read: sheet two, row B and column 4.

5.4.1.4 The specific types of equipment in the Suggested Equipment column are acceptable for service and provided as a guide in selecting suitable equipment; instruments having operating characteristics equal to or better than those indicated may be substituted. Refer to Table 5.1

Table 5.14 - Test Equipment

ITEM	MINIMUM USE SPECIFICATION	EQUIPMENT
DC Power Supply	Adjustable 0-20 VDS	-
Oscilloscope	100 MHz Band Width	TEK-465
DMM	0.1% DCV	Racal-Dana 4000
Counter	.1 Hz Resolution 10 MHz Ext. Reference Input	Racal-Dana 9000
Logic Clip		Best Source
Logic Probe		Best Source
Logic Comparator		Best Source
Logic Pulser		Best Source
Logic State Analyzer		Best Source
Simulator		Best Source
Emulator		Best Source
Controller	Or Equivalent	HP 9825

5.4.2 Software Troubleshooting.

5.4.2.1 Software and hardware problems may create the same symptoms but the cause may not be related. To isolate this problem, a list of General and Remote Error messages is supplied in Table 5.15. The general error messages numbered 0 to 9 apply to local and remote operations. The messages numbered 10 to 13 apply to GPIB operation only.

Table 5.15 - General and Remote Error Messages

Error Message No.	Error Message
	GENERAL ERROR MESSAGES
1	Not in the DC function, 0.1 range when executing DIGITAL ZERO command.
2	Attempting to execute DIGITAL ZERO command with an input voltage applied or the input open-circuited. Connect a short across input terminals and repeat DIGITAL ZERO command.
3	The microprocessor's on-board RAM is defective (U35 on the motherboard).
4	The contents of the non-volatile memory have been disrupted, therefore the instruments calibration should be verified.
5	A digitizer offset greater than 1000 digits was measured during execution of DIGITAL ZERO command
6	Percent Deviation of ≥ 1010% while in the Percent Function.
7	The RAM is defective, U22 and/or U31 on the motherboard.
8	An attempt was made to store a overload reading to a register inside the DMM or an attempt was made to store > 99.5959 hours into a Time function register.
9	An attempt was made to recall a program setting from the program buffer before setting was stored to the program buffer.
	GPIB ERROR MESSAGES
10	Recall of a constant whose value is empty set, for example - sending an "L7" command to a DMM will cause this error if the LOW, AVERAGE, and HIGH constants are the empty set (no readings taken yet.)
11	Triggered too fast or too often.
12	Syntax error during GPIB programming.
13	Option not installed.

5.4.3 Hardware Troubleshooting.

5.4.3.1 To service hardware, it is important to know the normal operation of the DMM. The block diagram in Figure 5.5 is presented as an overview to aid familiarization of the electrical configuration and Figure 5.4 indicates the test point on the parts layout of the mainframe PCB assembly. The schematic drawings in Section 6 complete the necessary details required to troubleshoot the DMM.

5.4.3.2 The DC voltages distributed throughout the DMM are a reliable status indicator and any deviation from normal can be readily observed. Typical operating voltages are supplied in Table 5.15 for the major circuits on the PCB. The left column names the circuits and the instructions are listed across the top. The chart information progresses from left to right. Using the circuit listing 'DIGITAL SUPPLY' for example, it reads:

a. Required voltage column reads +5VA and +5VB.

b. Parts Lay-out Reference Column: A guide to test-point locations.

c. Meter Probe column specifies the test-point connection. It reads Positive TP13 and Negative common TP5.

Table 5.16 - Power Supply Voltage Checks (Page 6-5)

Tests → / ↓ Circuit	Required Voltage DC ±10%	Parts Layout Ref.	Meter Probes Pos. Neg.	Reading OK	Move Probe To →	Move Probe To →	Move Probe To →	AC Reading
Digital Supply	+5VA	Fig. 5.8	Pos. TP13 Neg. TP5	No Next →	U50-IN No →	CR14, Cath. No →	→	Term 7 & 9 Power Trans.
	+5VB	Fig. 5.8	Pos. TP14 Neg. TP5	No Next →	U51-IN No →	CR15, Cath. No →	→	Term 7 & 9 Power Trans.
Non-Voltile Memory	+9V Un-Reg.	Fig. 5.8	Pos. CR14C Neg. TP5	No Next →	(Note: When +5VA or B OK, Then +9V OK) →			Term 7 & 9 Power Trans.
Analog	(+30V)	Fig. 5.8	Pos. CR22 Neg. TP12	No Next →	CR22, Cathode (+30V) No →	Lower Side R81 (+36V) No →	CR20+ (+36V) No →	Term 10 & 16 Power Trans.
Analog	(−30V)	Fig. 5.8	Pos. CR25 Neg. TP12	No Next →	CR25, Anode (−30V) No →	Left Side of R82 (−36V) No →	CR20− (−36V) No →	Term 10 & 16 Power Trans.
Isolator	+36V Un-Reg.	Fig. 5.8	Pos. CR20+ Neg. TP12	No Next →	(Note: When +30V OK, Then +36V OK) →			Term 10 & 16 Power Trans.
	−36V Un-Reg.	Fig. 5.8	Pos. CR20− Neg. TP12	No Next →	(Note: When −30V OK, Then −36V OK) →			Term 10 & 16 Power Trans.
AC-DC Ohms Op-Amps	+12V Un-Reg.	Fig. 5.8	Pos. U19 Pin 16 Neg. TP12	No Next →	U48-IN No →	CR-16+ No →	→	Term 11 & 15 Power Trans.
	−15V	Fig. 5.8	Pos. Can AR6 Neg. TP12	No Next →	No → U49-IN	No → CR16−	→	Term 11 & 15 Power Trans
Relay Drive	+12V Un-Reg.	Fig. 5.8	Pos. CR18-Cath. Neg. TP12	No Next →	No →	No →	No →	Term 12 - 14 Power Trans.
A-D Converter	+8V	Fig. 5.8	Pos. U33 Pin 16 Neg. TP12	No Next →	U52-IN No →	→	→	Term 12 - 14 Power Trans.
Non-Vol Memory Battery	+3V	Fig. 5.8	Pos. BT1-Pos. Neg. TP12	No Replace				
DC Supply	+5V	Fig. 5.8	Pos. CR21-Pos. Neg. TP12	No Next →	Pos. CR14 Cath. +9V. No →	→	→	Terminals 7 & 9 Power Transformer

5.4.3.3 When a voltage problem develops, (which usually alters the performance of the DMM, the mean-time-between failures (MTBF) indicates that capacitor failure can most often be the cause for the failure (filter or bypass). Therefore, whenever the DC voltages are below normal, the capacitors in that circuit should be examined as a possible fault source. For catastrophic power supply failures (smoke is evident), place a current limiter in series with the AC line. A lamp with half the unit rated wattage, in series with the line, will limit the current drain to a safe value, permitting service to be conducted.

5.4.3.4 Voltage problems are most often caused by temperature-related component failure, usually accompanied by an increased current drain and excessively high temperature at the specific component. Tracing the symptom can be simplified with conventional bench equipment listed next:

a) AC inline ammeter (mid-scale should read average current drain.)

b) Temperature probe (Racal-Dana T10).

c) Can of Cool-it or Freeze-it spray coolant. When a voltage problem develops, the voltage drop follows an increased current drain and excessive temperature increase at the faulty component. Spray the suspected component with cool-it and note the voltmeter and ammeter readings.

5.4.3.5 Digital debugging or troubleshooting procedures require additional test equipment compared to conventional electronic service. The digital test equipment listed in Table 5.1 is representative of the equipment available for digital and microprocessor service, although preference remains with the individual technician. Only a brief description of each unit is presented for the technical center needing digital equipment:

a) LOGIC CLIP: Instantly displays the logic states of all DIP pins (TTL or DTL). The LED's follow the logic state changes (level changes).

b) LOGIC PROBE: Permits examination of one pin, indicating if the state is high or low. The probe blinks to indicate the presence of a pulse train.

c) LOGIC COMPARATOR: Clips on to a powered TTL chip and displays any logic state difference between the IC under test and a reference IC. Logic differences are identified to a specific pin.

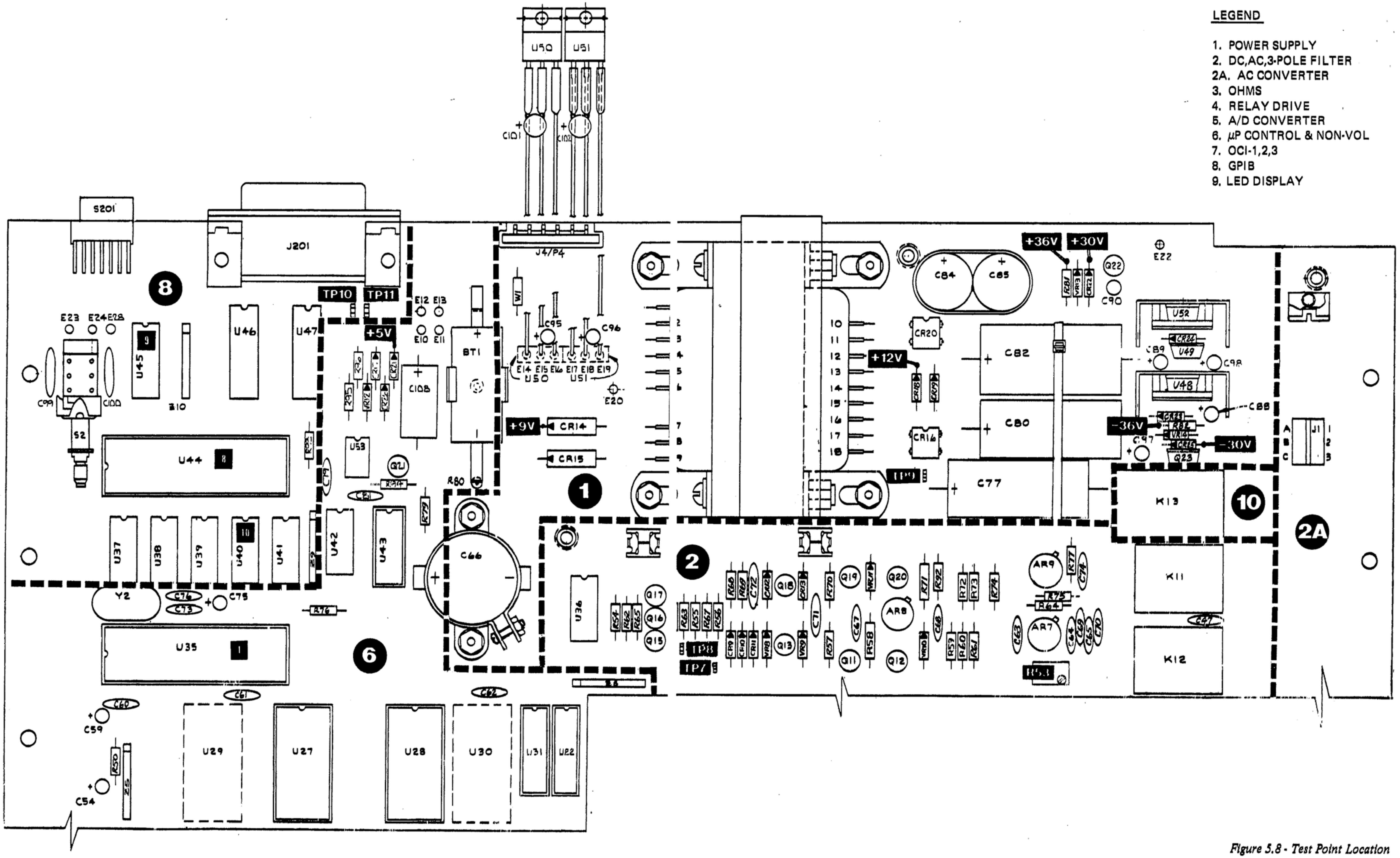
d) LOGIC PULSER: This probe injects a narrow pulse into the circuit to determine if a gate is working. The gate will switch state.

e) LOGIC STATE ANALYSER: A CRT display device that can exhibit up to 32 channels of digital input. The data words in process can be examined in relation to time and events.

f) SIMULATOR: This system employs software to replace the hardware functions. The software program will generate the same outputs as the hardware device.

g) EMULATOR: The emulator executes the processor programs in real time by connecting the emulator DIP connector into the MPU socket and inserting the MPU into the emulator probe. This device is usually a service feature of the Chip manufacturer.

5.4.3.6 Troubleshooting practices basically require the individual's logical deductions to solve product failure. The cases presented in Troubleshooting Table 5.17 list the causes of the problem, the probably cause generating the symptoms and Suggested Corrections. The test equipment employed is left to the individual's preference.



LEGEND

1. POWER SUPPLY
2. DC,AC,3-POLE FILTER
2A. AC CONVERTER
3. OHMS
4. RELAY DRIVE
5. A/D CONVERTER
6. µP CONTROL & NON-VOL
7. OCI-1,2,3
8. GPIB
9. LED DISPLAY

Figure 5.8 - Test Point Location

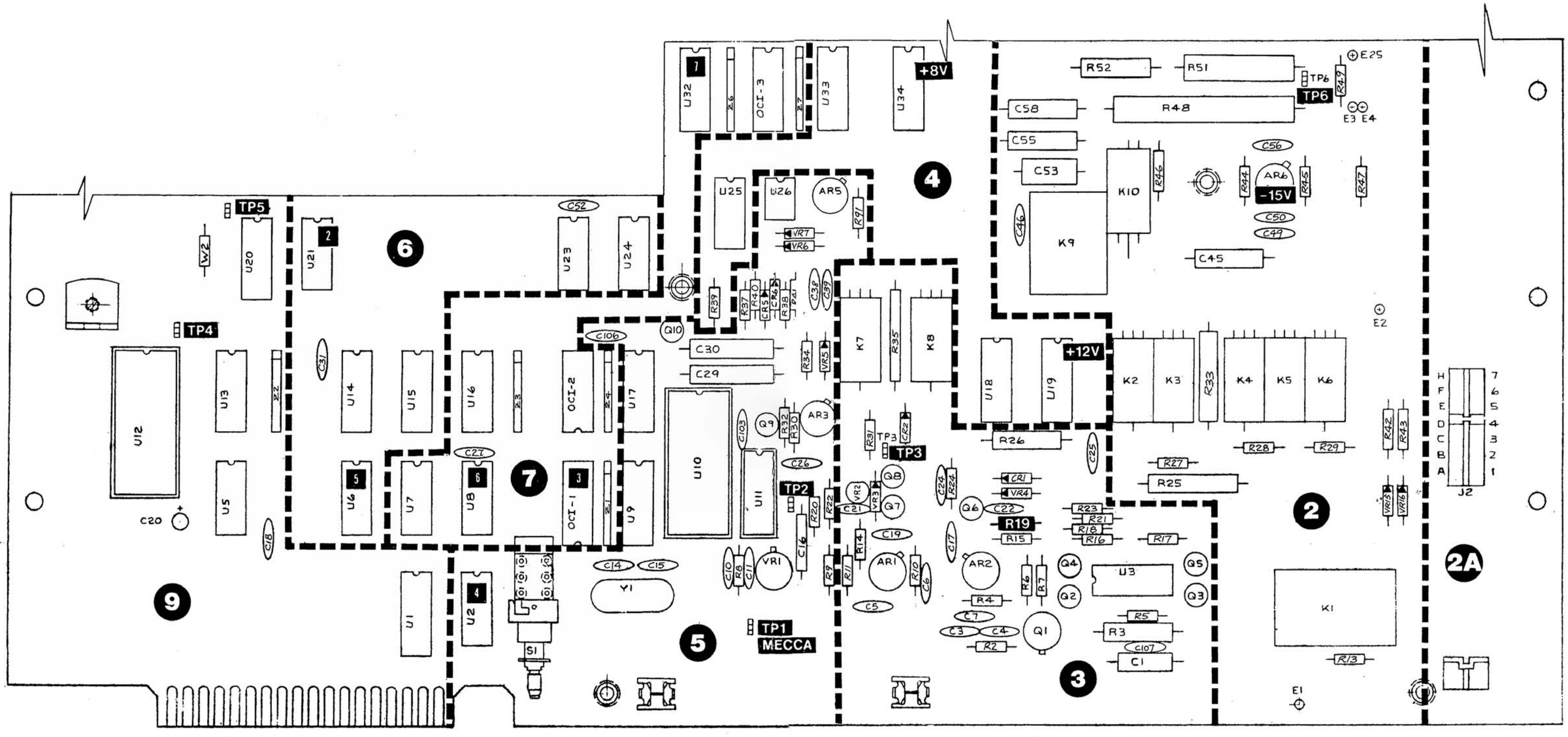


Figure 5.8 - Test Point Location continued

Table 5.17 - Troubleshooting Examples

SYMPTOMS	PROBABLE CAUSE	SUGGESTED CORRECTIONS
EXAMPLE–A		
DMM displays "5004" during power-up	U20 data buffer may be defective.	Replace U20
DMM displays "5003" during power-up	U28 ROM may be defective.	Replace U28
EXAMPLE–B		
DMM displays model number and/or error message, then fails to proceed. (Hangs-up).	µP unable to control inguard or outguard logic; or µP unable to read from logic using 74LS367 buffers.	Scope address decoder outputs U14 pins 15, 14, 13, 12, 11, 10 and 9 or U15 pins 14 and 13. Watch for narrow, negative-going pulses which indicate that the µP is continually waiting for some hardware events or is trying unsuccessfully to initiate a hardware event. The affected address decoder output gives an indication of the hardware involved.
EXAMPLE–C		
DMM continues to take readings when in "SINGLE" or "RECALL" mode.	µP receiving NMI (non-maskable interrupt) on U35-6	Verify operation of U2 interrupt and associated circuitry
	OR	
	loss of "read control" signal somewhere between µP and A/D converter	Check read control signal as it propagates from U35-15 µP chip through OCI-3 to U10-26 digital control chip.
EXAMPLE–D	Defective Dc power supply in Analog Section	Verify power supplies and replace components as necessary.
Function LED's correspond to selected function but relays don't always change state to match newly selected function.	Register Load Hardware (U33-U34) defective.	Alternately press front panel DC and AC keys rapidly and verify the output waveforms from OCI-3 all pins. The signal will swing between 1-1/2 V and 6-1/2 V minimum. They should track the driving waveforms which are partially shown in Table 5.16 Performance tests. Also, verify the operation of U32, U33 and U34. Verify the presence of strobe pulse on U33/U34-1 after last clock pulse on U33/U34-3

Table 5.17 - Troubleshooting Examples continued

SYMPTOMS	PROBABLE CAUSE	SUGGESTED CORRECTIONS
EXAMPLE–E DMM ignores keyboard.	Key on keyboard is already "pressed" (shorted)	Troubleshoot keyboard rows and columns switch operation
	OR	
	μP unable to read keyboard status from keyboard three-state buffer.	Verify the operation of U13-keyboard buffer.
	OR	
	Defective GPIB hardware causes DMM to go to "remote" at power-up	Verify that "remote" LED is not lit after completion of power-up sequence. If LED is lit, replace U44, GPIA.
EXAMPLE–F "ERROR 5" displayed during digital zero command	U26 - M/Z switch failing to switch AR5-3 to zero volts during digital zero.	Verify a logical '1' on U26-2 during digital zero. If not present, see suggested corrections for Example–D, otherwise verify other analog and digital signals on U26.
	OR	
	A/D converter IC's are suspect	Replace U10 and/or U11.
	OR	
	A/D output signals lost as they propagate through U17-U9 digitizer drives, OCI-1/2 op-to couplers, and U16 data driver.	Troubleshoot chips, checking for "stuck" levels at each stage.

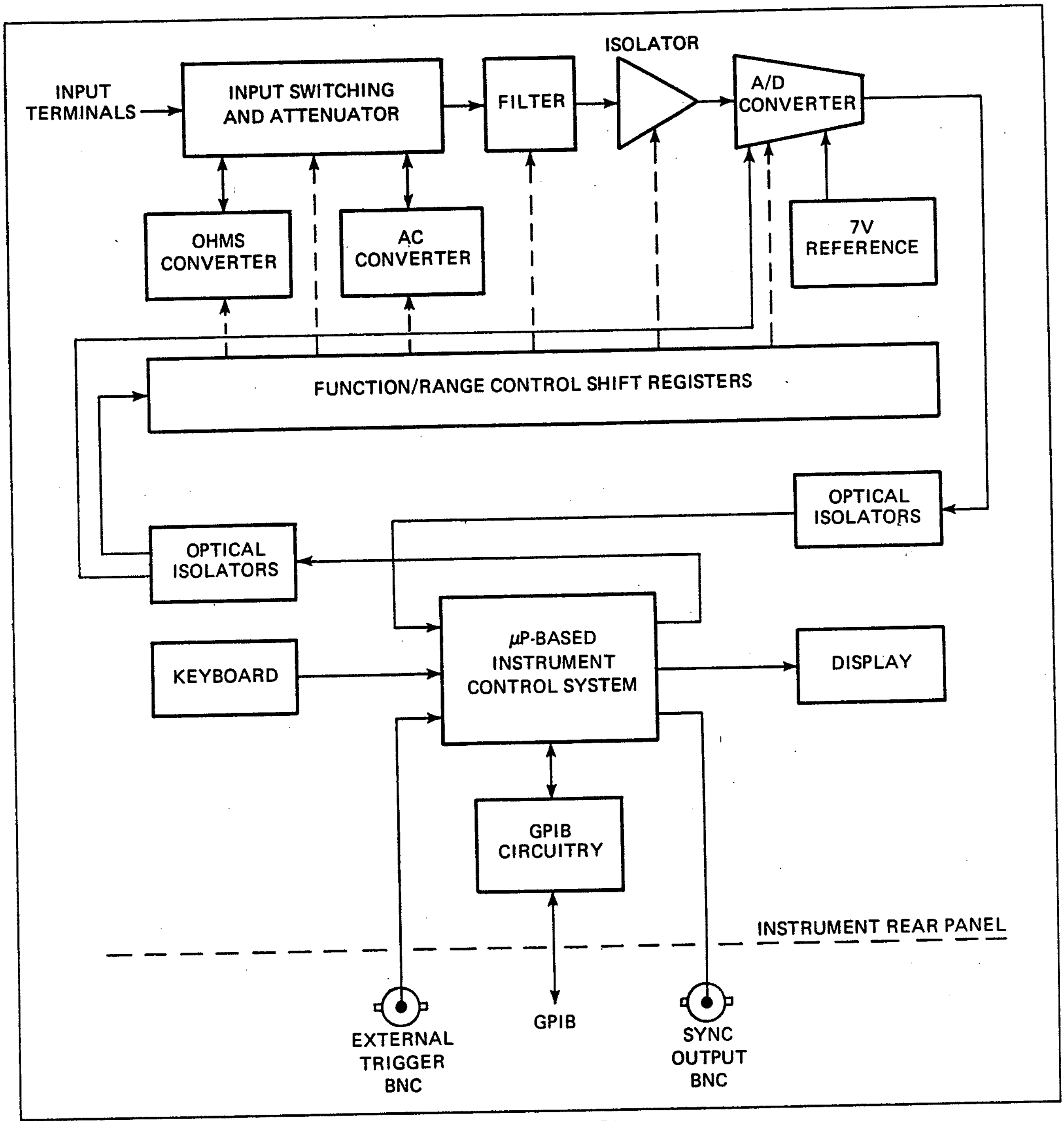


Figure 5.9 - DMM Block Diagram

5.4.4 Troubleshooting Performance Tests.

5.4.4.1 The performance tests are designed to isolate a malfunction to a replaceable module or printed circuit board. In some cases where the printed circuit board is large and complex, the test is designed to isolate the malfunction to a functional area of the board.

5.4.4.2 Both the unit and subassembly performance tests present setup instructions—step by step for monitoring the circuit under test, and performance standards listed as voltage levels or oscilloscope waveforms. Parts layout drawings are provided to aid in locating the test points on the assembly board.

5.4.4.3 Test points called out in the performance tests may be actual physical test points provided as convenient test points or they may simply be circuit locations such as the end of a resistor or the emitter of a transistor. In either case the test points appear in the performance test tables as black squares.

5.4.4.4 Note that the test points are numbered sequentially from the start of the performance tests and progress to the end. The performance standard for each test point is shown in the table if it is a voltage standard; the waveform standards are provided on waveform illustration pages immediately following the performance test table. The numbered test points refer to square black test point flags **1** appearing on the assembly drawing in the Drawing Section (6).

5.4.4.5 To perform subassembly performance tests refer to the appropriate test table, perform the preliminary test setup presented as the first few steps of the test. When the setup is complete proceed with test and verify that the measurement at each test point is within tolerances called for in the performance standard column of the test. If at any point in the test you do not obtain the required voltage or signal refer to the appropriate schematic to determine the area of the malfunction. Resort to conventional troubleshooting methods to identify the faulty component or circuit. The term conventional troubleshooting methods as used here means checking individual semiconductors, resistors and capacitors in and around the area of malfunction.

WARNING

These servicing instructions are for use by qualified personnel only. To avoid electric shock, do not perform any servicing other than that contained in the instructions unless you are qualified to do so.

5.4.4.6 Tables 5.18 through 5.20 present the unit performance tests. Note that the tables contain performance standards for voltage measurements and waveforms. The tolerance required for troubleshooting is looser than operating tolerances because the technician is generally looking for the presence of the signal rather than an exact high tolerance standard. This allows the use of a much broader range of test equipment and also allows the use of test equipment that is not subject to high accuracy calibration requirements.

5.4.5 Battery Replacement For Non-Vol Circuit.

5.4.5.1 During power-down periods when the DMM is not AC line powered, a Lithium battery (BT1 located in section 1) maintains the required voltage to the Non-Volatile memory circuit, which includes the CMOS RAM U43. When the voltage drops below 2.3V, the RAM will lose its CAL constants. This causes the "ERROR 4" message to be displayed next time the DMM is powered-up.

5.4.5.2 It is important to recognize that the displayed error message indicates that the contents of the Non-Vol memory were disrupted and most often indicates a discharged battery. If the battery voltage to U43-16 with power-down exceeds 2.3V, other components in the circuit may be at fault.

5.4.5.3 STEPS TO REPLACE BT1 BATTERY.

a) Apply power to the DMM. Verify that it completes the power-up sequence listed in paragraph 3.2.2.

WARNING

During removal of the bottom guard-shield plate, care must be taken that the non-volatile memory battery supply (BT-1) is not short-circuited, losing all CAL constants stored in memory. When the guard-shield is freed, lift directly away from or at right-angle (orthogonal) to the PCB. Do not slide the shield over the PCB.

b) CAUTION: The DMM is still powered-up. Use a battery powered or un-grounded soldering iron to unsolder the battery tabs from the motherboard and remove the old battery.

c) Observe polarity and install the new battery in the same position.

WARNING

Lithium batteries may explode if short-circuited, recharged, disassembled, heated, disposed of in fire, or exposed to temperatures above 90°C. Battery leakage may forewarn a problem.

5.4.5.4 Preventative Maintenance: Use the following procedure to check the battery condition:

a) Turn-off the AC power to the DMM.

b) Wait 30 seconds.

c) Measure the voltage drop with a one millivolt resolution DVM across R80, the 1 Kohm resistor in series with the battery.

d) The voltage drop across R80 should be less than 20 mV (battery drain 20 μA).

5.4.5.5 Suggested Battery Replacement Interval can be determined from Figure 5.10. It is supplied as an aid to determine how often the Lithium battery, BT1, should be replaced. Notice that the worst-case battery drain occurs if the instrument is stored at high temperatures with the power off (3 year replacement interval). For most applications, a 4 year replacement interval is suggested.

5.4.6 Lithum Battery Safety Precautions

5.4.6.1 Do not store the batteries in areas where the ambient temperature exceeds 90^{o} centigrade.

5.4.6.2 Verify that the discarded battery is completely discharged. Connecting a 10 ohm one-watt resistor across the terminals for 24 hours will completely discharge the battery.

5.4.6.3 Return the completely discharged battery to your local Racal-Dana Representative, service depot or locally assigned disposal areas.

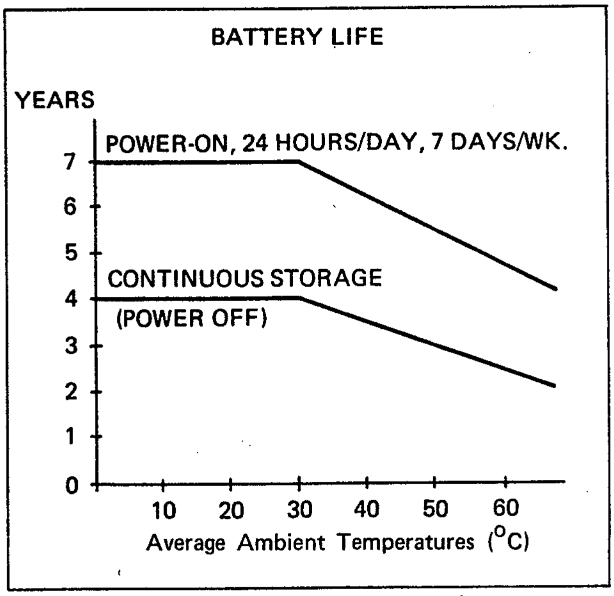


Figure 5.10 - Battery Life Graph

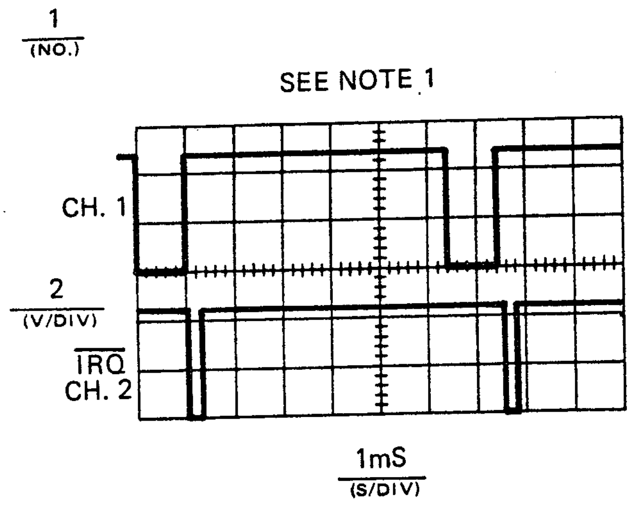
Table 5.18 - **Digital Section Performance Test**

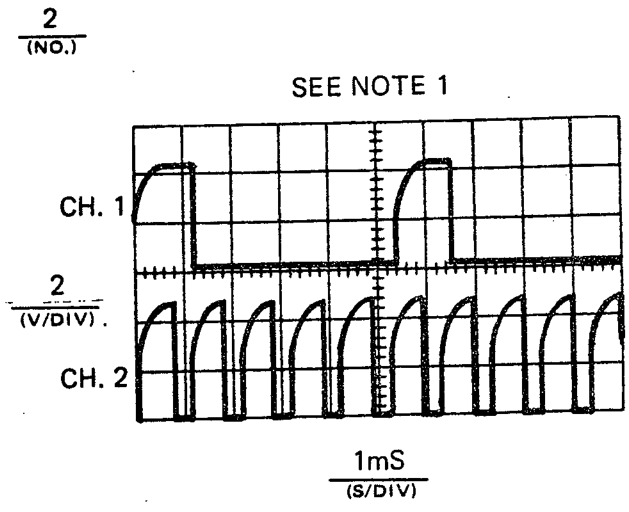
Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Using conventional techniques, the Digital Section can only be tested to the point where certain "Knowns" can be verified. If the proper waveforms are not observed, the nearest Racal-Dana serivce center should be contacted.					
All measurements in this table are referenced to TP4, Digital Common. Power Switch: ON				Test Points Shown on Figure 5.4	
Disconnect any cables connected to Rear Panel GPIB and BNC Connectors	+5 VA +5 VA +5 VB $\overline{\text{Reset}}$ $\overline{\text{NMI}}$	 U35 Pin 40 U35 Pin 6	 1 1		+5V ± .25 VDC +5V ± .25 VDC +5V ± .25 V +2.5V to +5.25V with no excursions below +2.5V
Set Scope Trigger To Internal, Channel 1, + Slope	μP Clock E	U21 Pin 11	2		Waveforms #7, Ch. 1
	Inverse Signal $\overline{\text{E}}$	U21 Pin 10	2		Waveforms #7, Ch. 2
	Address Bus	U35 Pins 9 to 20 and 22 to 25	1		See Note Below
	Data Bus	U35 Pins 26 to 33	1		See Note Below
	VMA	U35 Pin 5	1		See Note Below
	R/$\overline{\text{W}}$	U35 Pin 34	1		See Note Below
	W/$\overline{\text{R}}$	U21 Pin 8	2		See Note Below
Scope Trigger Set To: Internal, + Slope, Channel 1	Digit Strobe Sync D6 (After Opto-isolation)	OCI1 Pin 11	3		Waveforms #2, Ch. 1
	1 KHz (After Opto-isolation) (approx. .83 KHz in 50 Hz Machine)	OCI1 Pin 14	3		Waveforms #2, Ch. 2
Note: These waveforms are asynchronous TTL signals. If the signals are always high or low at this point, it is an indication of a Fault.					

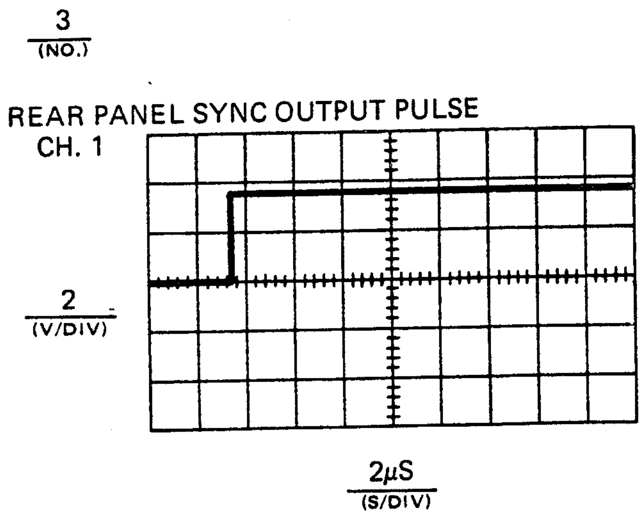
Table 5.18 - **Digital Section Performance Test continued**

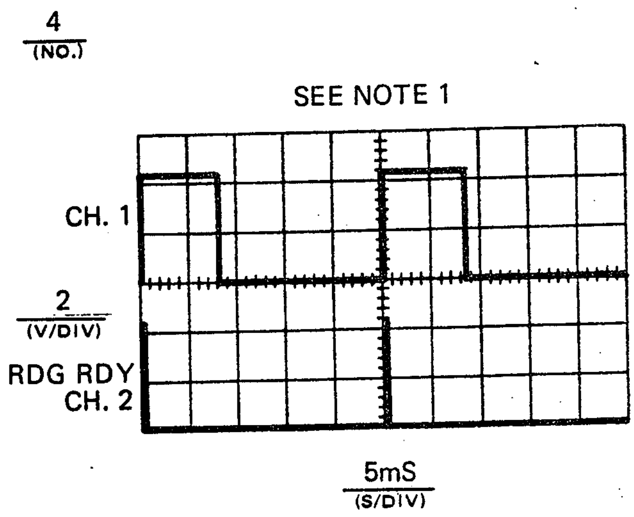
Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Instrument in "Hold" Mode (Press "SINGLE" Key on Keyboard)	Clock to Interrupt - Control FF	U2 Pin 11	4		Waveforms #1, Ch. 1
Scope Trigger Set To: Internal, – Slope, Channel 1	$\overline{\text{IRQ}}$ Input to μP	U35 Pin 4	1		Waveforms #1, Ch. 2
Instrument in "Hold" mode (Press "SINGLE" Key on Keyboard) Scope Trigger Set To: Internal, – Slope, Channel 1	$\overline{\text{DSPE}}$	U6 Pin 8	5		Waveforms #5, Ch. 1
DMM Set to Internal Trigger (Press "Track" Key) 4 1/2 Digit Mode (Toggle "RESOL" Key if required)	$\overline{\text{End of Conversion}}$ (After Opto-isolation and Schmitt Trigger Inversion)	U8 Pin 11	6		Waveforms #4, Ch. 1
Scope Trigger Set To: Internal, + Slope, Channel 1	Rdg Rdy (Reading Ready)	U8 Pin 9	6		Waveforms #4, Ch. 2
DMM Set to Internal Trigger (Press "Track" Key) 4 1/2 Digit Mode (Toggle "RESOL" Key if required)	Sync Output	Sync Output BNC (Rear Panel)	Rear Panel BNC		Waveform #3
Scope Trigger Set To: Internal, – Slope, Channel 1 Alternately Press "10" and "100" Range Keys at a Rapid Rate Scope Trigger Set To: Internal, + Slope, Channel 1	CLK	U32 Pin 7	7		Waveforms #6, Ch. 1
	Strobe	U32 Pin 2	7		Waveforms #6, Ch. 2

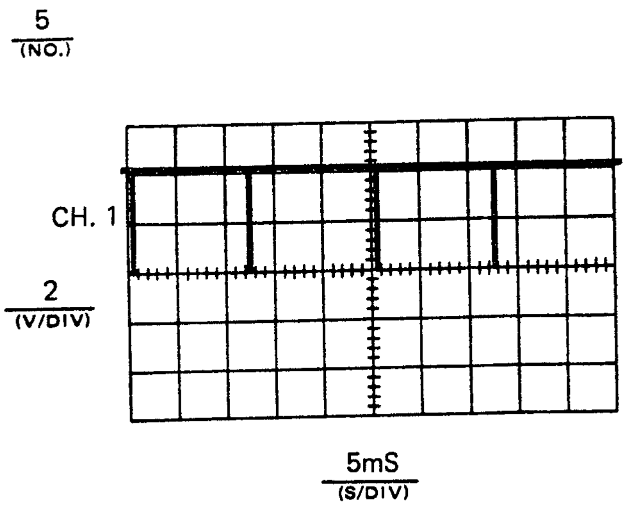
Table 5.18 - Digital Section Performance Test continued

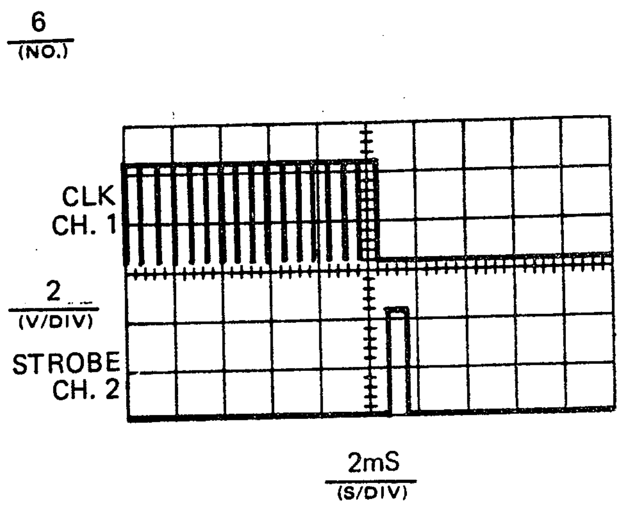












NOTE 1 WAVEFORMS ARE SHOWN FOR A 60 Hz UNIT. WAVEFORMS TAKEN FROM A 50 Hz UNIT WILL BE 10% LOWER IN FREQUENCY.

Table 5.18 - Digital Section Performance Test continued

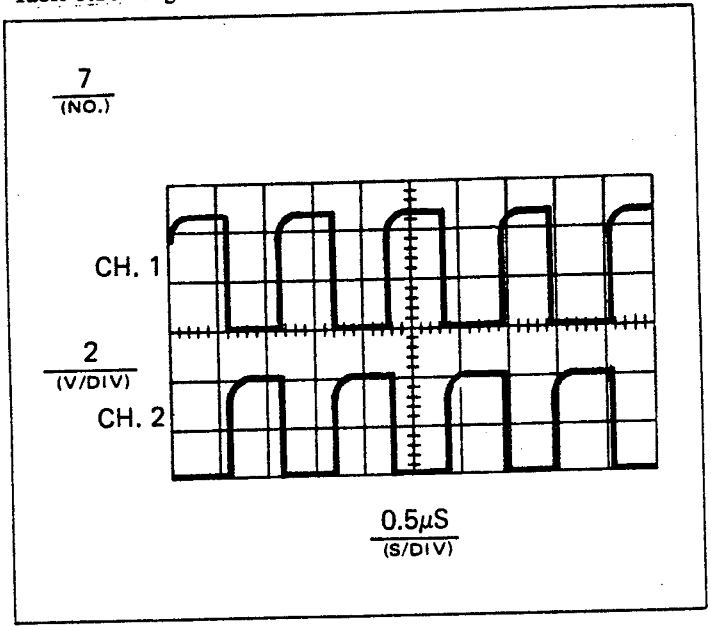


Table 5.19 - GPIB Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Set All Rear Panel GPIB Switches to their Lower Position. Turn DMM's Power Off and then On again.	All measurements in this table are referenced to TP4, Digital Common.				
Disconnect all Cables from GPIB Connector	GPIB Data/Control Lines	J201 Pins 1-11 and Pins 13-17		Rear Panel Connector	+2.5 to +3.7V
	68488 GPIB I/O Lines	U44 Pins 16-23, Pins 25,26 Pins 29-36	8		+2.5 to +5.25V
DMM in "HOLD" Mode (Press "SINGLE" Key) Set Scope Trigger to Internal, – Slope, Channel 1	$\overline{\text{ASE}}$	U45 Pin 1 and/or Pin 15	9		GPIB Waveform # 1
DMM set to Internal Trigger (Press "Track" Key) 4 1/2 Digit Mode (Toggle "RESOL" Key if necessary) Talk Only (Set Rear Panel "talk only" Switch to "up" position) Set Scope Trigger to Internal, + Slope, Channel 1	Momentary Output Holdoff Pulse from μP (1 per Reading)	U39 Pin 8	10		GPIB Waveform # 2

Table 5.19 - GPIB Performance Test continued

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
DMM Set to Internal Trigger (Press "Track" Key) 4 1/2 Digit Mode (Toggle "RESOL" Key if necessary) Talk Only (Set Rear Panel "talk only" Switch to "up" position) Set Scope Trigger to Internal, + Slope, Channel 1	RFD	U44 Pin 18	8		GPIB Waveform # 3
DMM Set to Internal Trigger (Press "Track" Key) 4 1/2 Digit Mode (Toggle "RESOL" Key if necessary) Talk Only (Set Rear Panel "talk only" Switch to "up" position) Set Scope Trigger to Internal, + Slope, Channel 1	RFD $\overline{\text{GPIRQ}}$	U44 Pin 18 U44 Pin 40	8		GPIB Waveform # 4 Channel 1 GPIB Waveform # 4 Channel 2

Table 5.19 - GPIB Performance Test continued

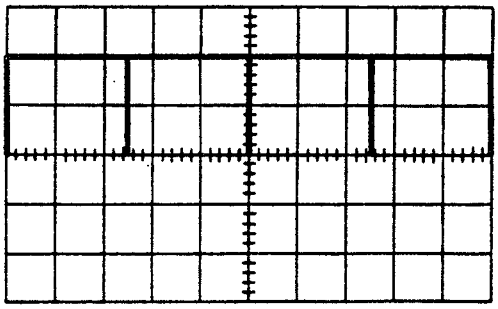
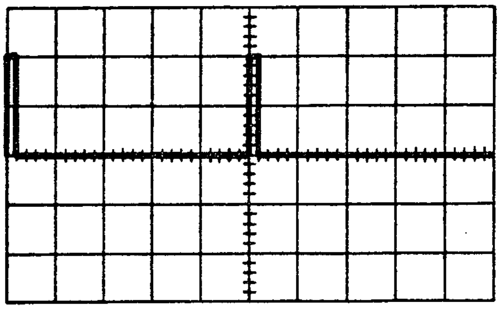
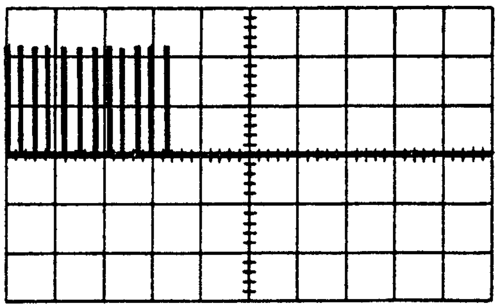
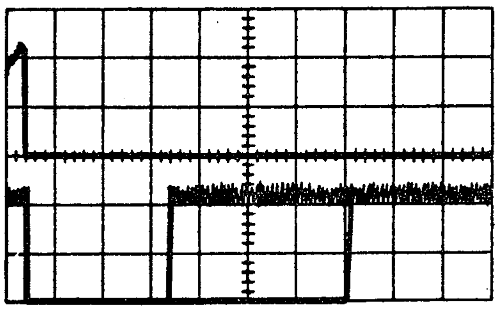
1 (NO.) CH. 1  2 (V/DIV) 5mS (S/DIV)	2 (NO.) CH. 1  2 (V/DIV) 5mS (S/DIV)
3 (NO.) CH. 1  2 (V/DIV) 0.5mS (S/DIV)	4 (NO.) CH. 1  2 (V/DIV) CH. 2 10μS (S/DIV)

Table 5.20 - Digitizer Performance Test

Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
All measurements made in this table referenced to "Mecca" TP1. Instrument in 0.1V Range DC,input shorted. Internal Trig. (Hit "Track" Key) Scope Trigger set to: Ch. 2, +, internal	D1 - D5	U10 Pins 3-8			Waveforms # 2-6
	D6	U10 Pin 8			Waveform # 1
Instrument in 0.1V Range DC,input shorted. Internal Trig. (Press "Track" Key) Scope Trigger set to: Ch. 1, +, internal	1 KHz Clock	U10 Pin 28			Waveform # 7
Instrument in 0.1V Range DC, input shorted, internal trigger (Press "Track" Key) Scope trigger set to: Ch. 1, +, internal	2.5 MHz Clock	U10 Pin 14			Waveform # 8
Instrument in 0.1V Range DC, input shorted, internal trigger (Press "Track" Key) Scope Trigger set to: Normal, +, internal	E.O.C.	U10 Pin 19			Waveform # 9
Instrument in 0.1V Range DC, input shorted, internal trigger (Press "Track" Key) Scope Trigger set to: Normal, +, internal	M.Z.	U10 Pin 20			Waveform # 10
Instrument in 1V Range DC, +2V in internal trigger (Press "track" key) Scope Trigger set to: Normal, –, internal	M.Z. Switch	U26 Pin 4			Waveform # 11
Instrument in 1V Range DC, –2V in internal trigger (press track key) Scope trigger set to: Normal, +, internal	M.Z. Switch	U26 Pin 4			Waveform # 12

Table 5.20 - **Digitizer Performance Test continued**

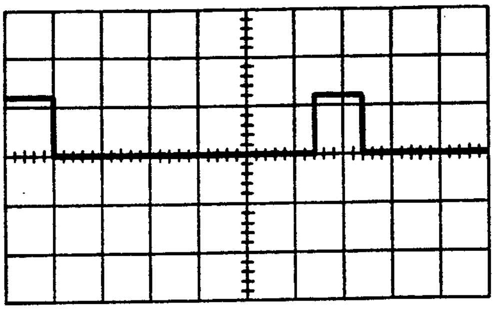
Input and Control Setting	Signal Nomenclature	Reference Designation	Test Point	Illustration Reference	Performance Standard
Instrument in .1V Range DC, input shorted, internal triggered (Press "track" key) + probe on: −probe on:	A-D Converter Reference Voltage	U11, Pin 10 Mecca TP-1			+7V ± 0.4V
Instrument in 0.1V Range DC, input shorted, internal trigger (Press "Track" Key) + Probe on: −probe on:	V_{STRG} (Auto-Zero Voltage)	AR3, pin 6			−2.6V ± 1V

Table 5.20 - Digitizer Performance Test continued

1 (NO.)

CH. 2 D6

5 (V/DIV)



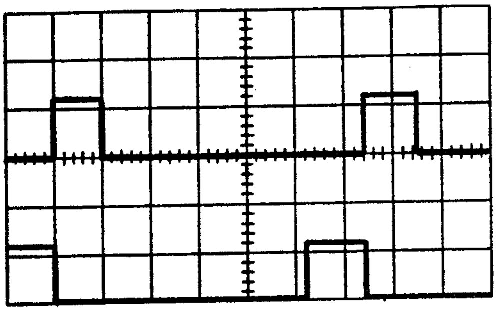
1 MS (S/DIV)

2 (NO.)

D1

5 (V/DIV)

D6



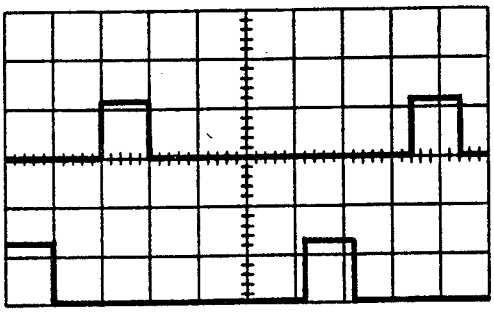
1 MS (S/DIV)

3 (NO.)

D2

5 (V/DIV)

D6



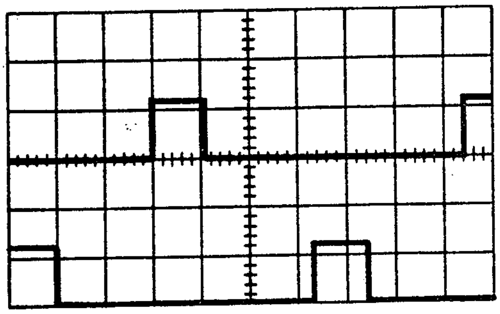
1 MS (S/DIV)

4 (NO.)

D3

5 (V/DIV)

D6



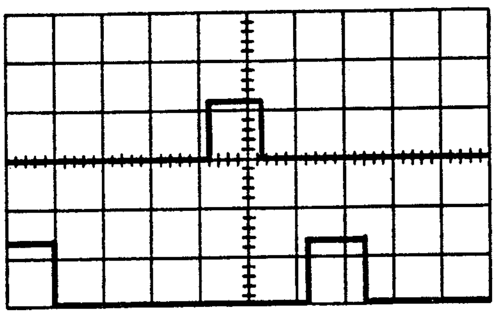
1 MS (S/DIV)

5 (NO.)

D4

5 (V/DIV)

D6



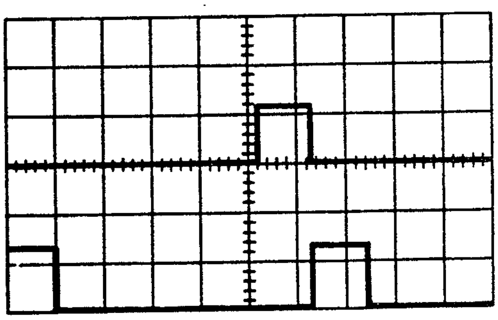
1 MS (S/DIV)

6 (NO.)

D5

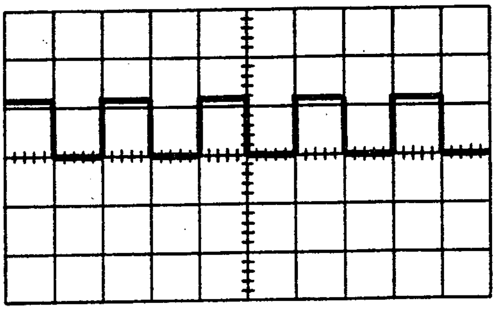
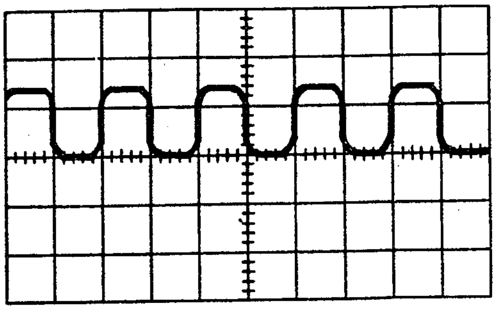
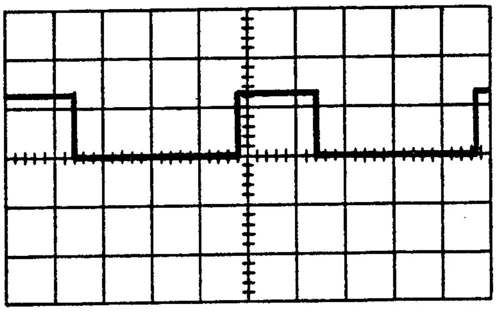
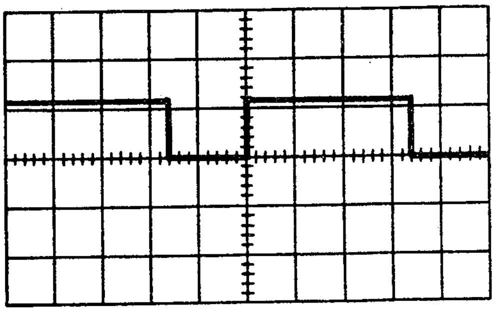
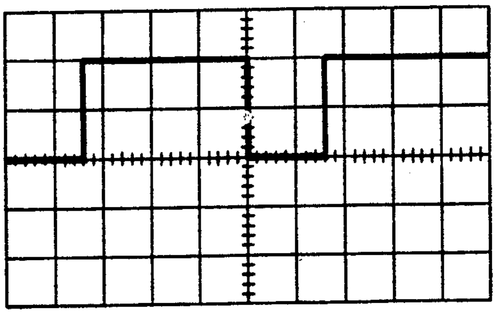
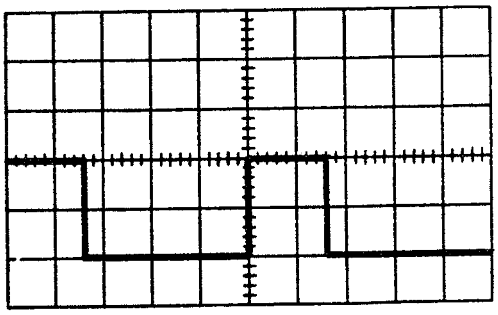
5 (V/DIV)

D6

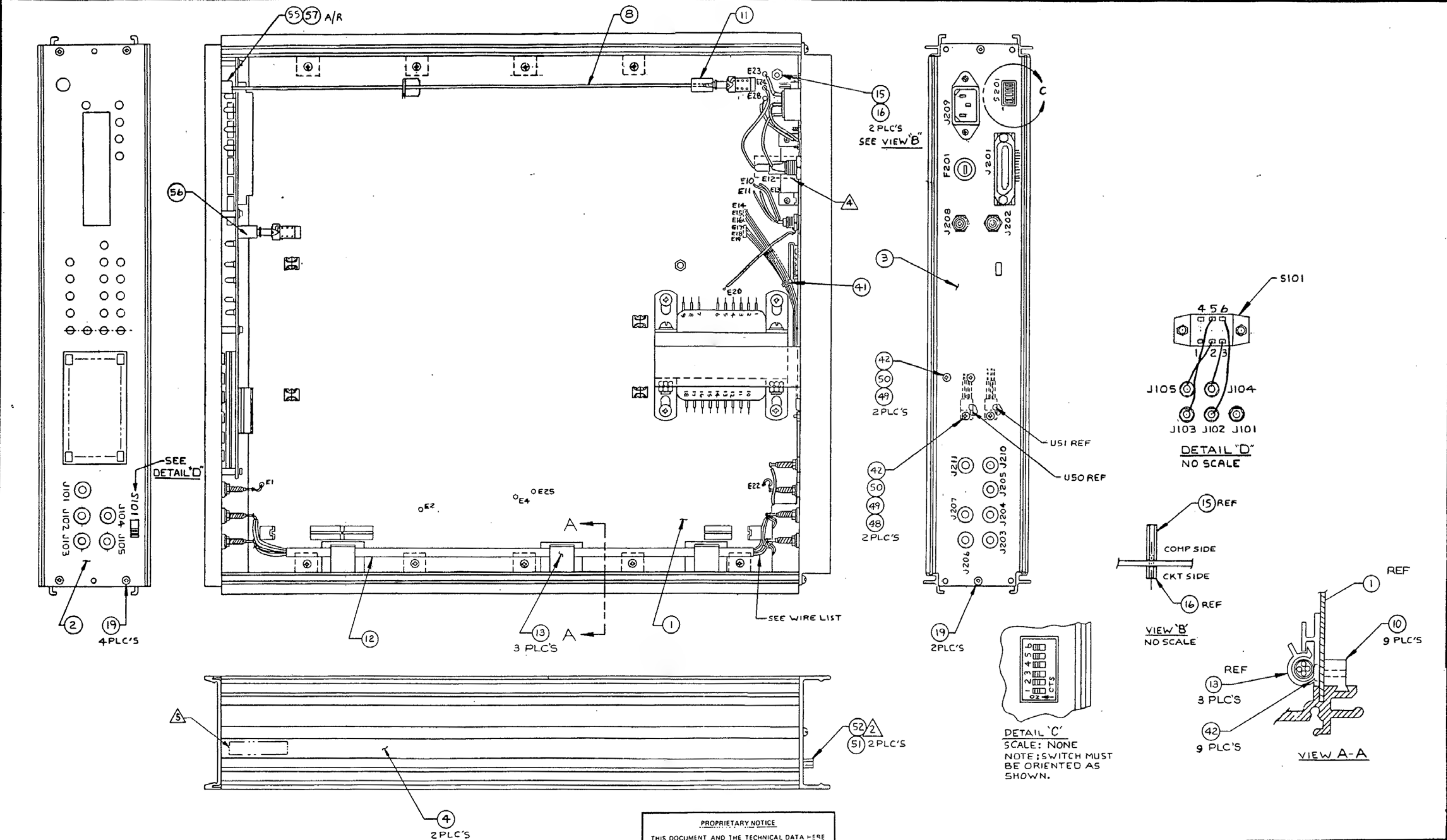


1 MS (S/DIV)

Table 5.20 - Digitizer Performance Test continued

7 (NO.) 1 KHz CLOCK 5 (V/DIV)  0.5 MS (S/DIV)	8 (NO.) 2.5 MHz CLOCK 5 (V/DIV)  0.2 μS (S/DIV)
9 (NO.) E.O.C. 5 (V/DIV)  50 MS (S/DIV)	10 (NO.) M.Z. 5 (V/DIV)  50 MS (S/DIV)
11 (NO.) M.Z. SWITCH 0V 1 (V/DIV)  50 MS (S/DIV)	12 (NO.) M.Z. SWITCH 0V 1 (V/DIV)  50 MS (S/DIV)

SECTION 6 DRAWINGS



5. FOR PROPER SIDE PANEL ORIENTATION RACAL-DANA P/N MUST APPEAR AT FRONT END OF INSTRUMENT.
4. INSTALL SHRINK TUBING OVER FUSEHOLDER AFTER WIRES ARE SOLDERED TO TERMINALS
3. SEE WIRE LIST FOR INDIVIDUAL WIRE LENGTHS & TERMINATION POINTS; USE SHRINK TUBING AS REQUIRED.
2. DISCARD LOCKWASHERS & WASHERS SUPPLIED WITH ITEM 52.
1. ASSEMBLY PROCESSES + PROCEDURES TO CONFORM TO RACAL-DANA STANDARD.

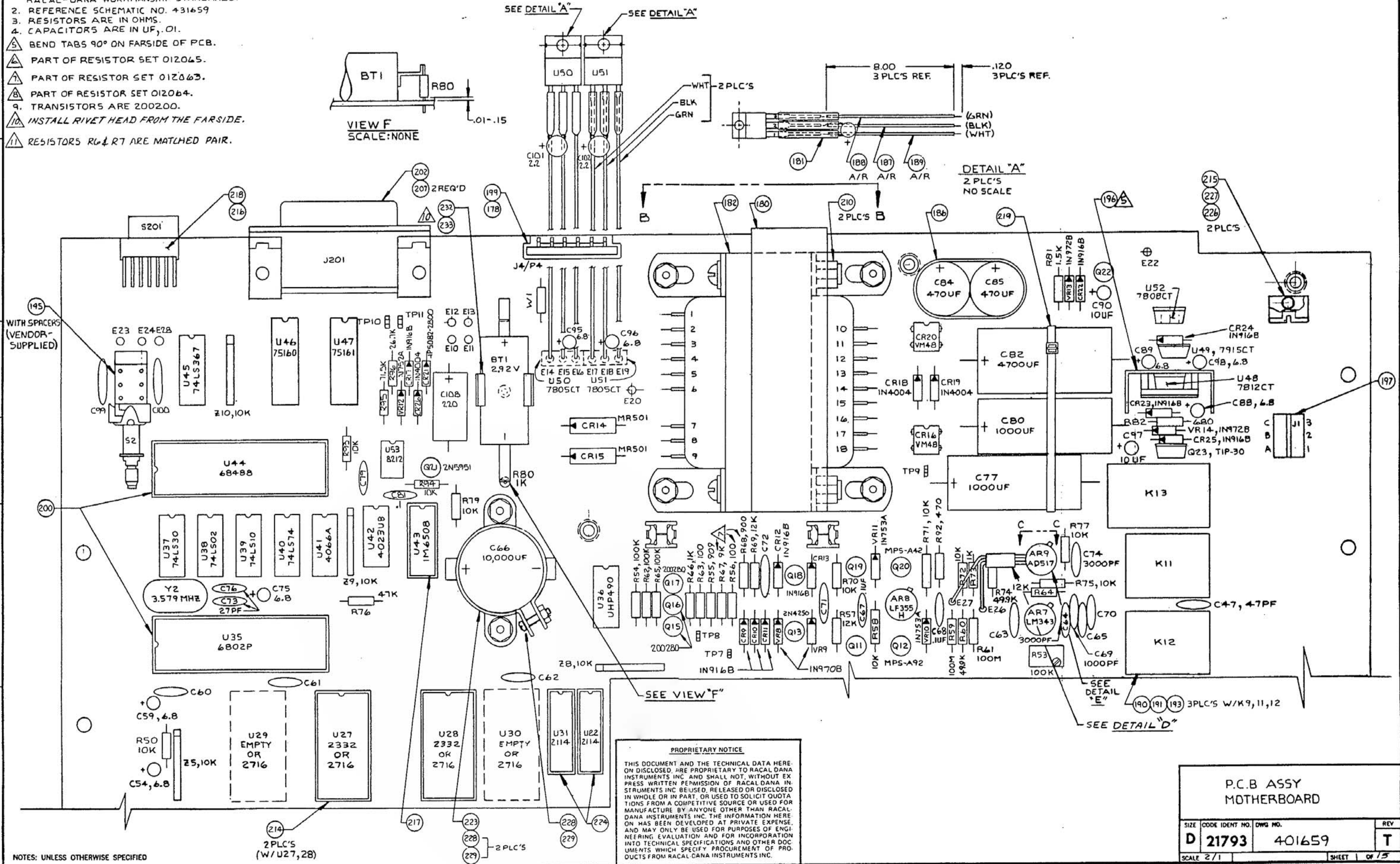
NOTES: UNLESS OTHERWISE SPECIFIED

CHASSIS ASSEMBLY

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	404136	J
SCALE NONE		SHEET 1 OF 7	

NOTE UNLESS OTHERWISE SPECIFIED

1. ASSEMBLY PROCESSES & PROCEDURES TO CONFORM TO RACAL-DANA WORKMANSHIP STANDARDS.
2. REFERENCE SCHEMATIC NO. 431659
3. RESISTORS ARE IN OHMS.
4. CAPACITORS ARE IN UF, .01.
5. ⚠ BEND TABS 90° ON FARSIDE OF PCB.
6. ⚠ PART OF RESISTOR SET 012065.
7. ⚠ PART OF RESISTOR SET 012063.
8. ⚠ PART OF RESISTOR SET 012064.
9. TRANSISTORS ARE 200200.
10. ⚠ *INSTALL RIVET HEAD FROM THE FARSIDE.*
11. ⚠ *RESISTORS R6 & R7 ARE MATCHED PAIR.*



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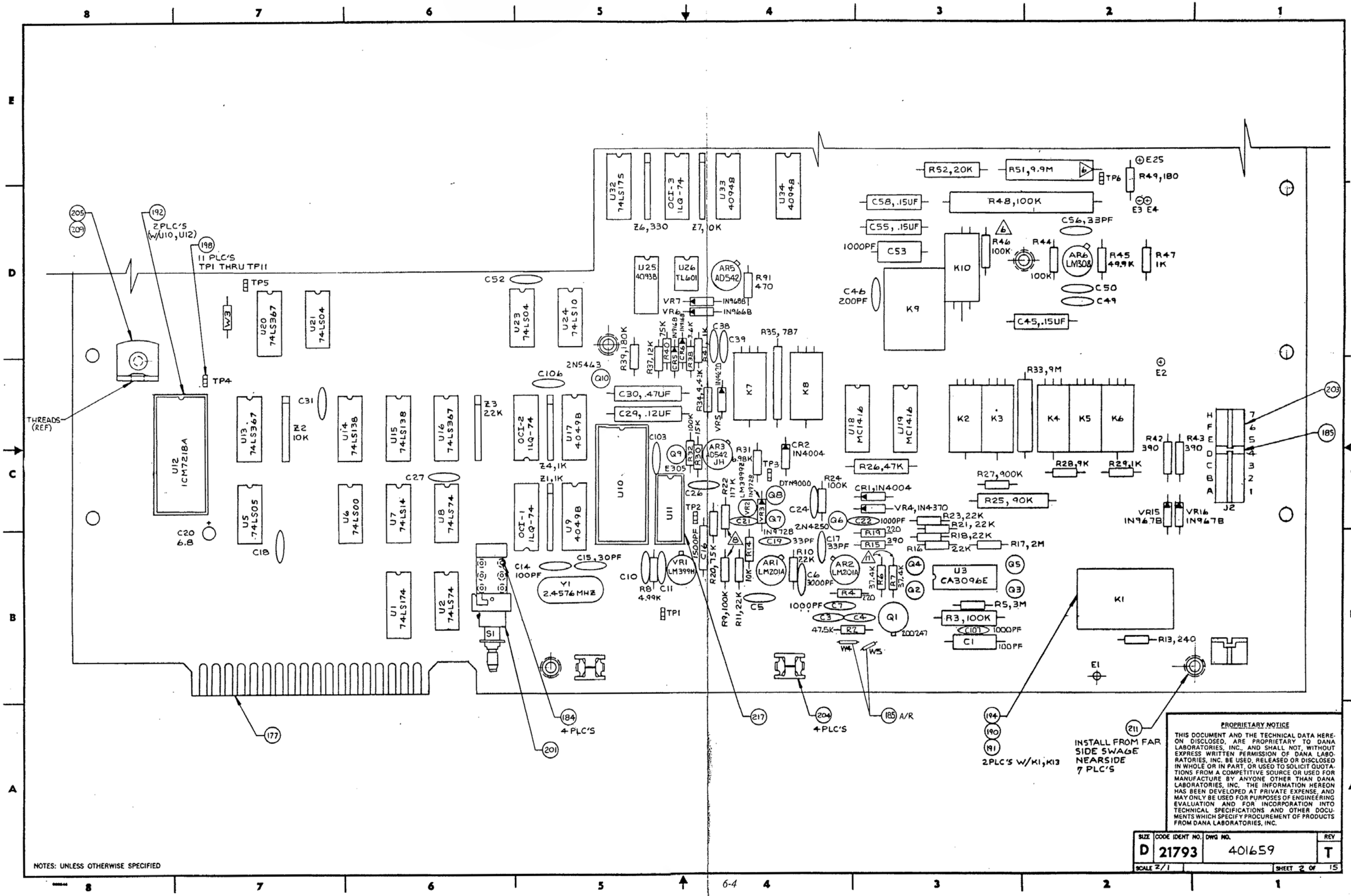
P.C.B ASSY
MOTHERBOARD

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	401659	T
SCALE 2/1		SHEET 1 OF 5	

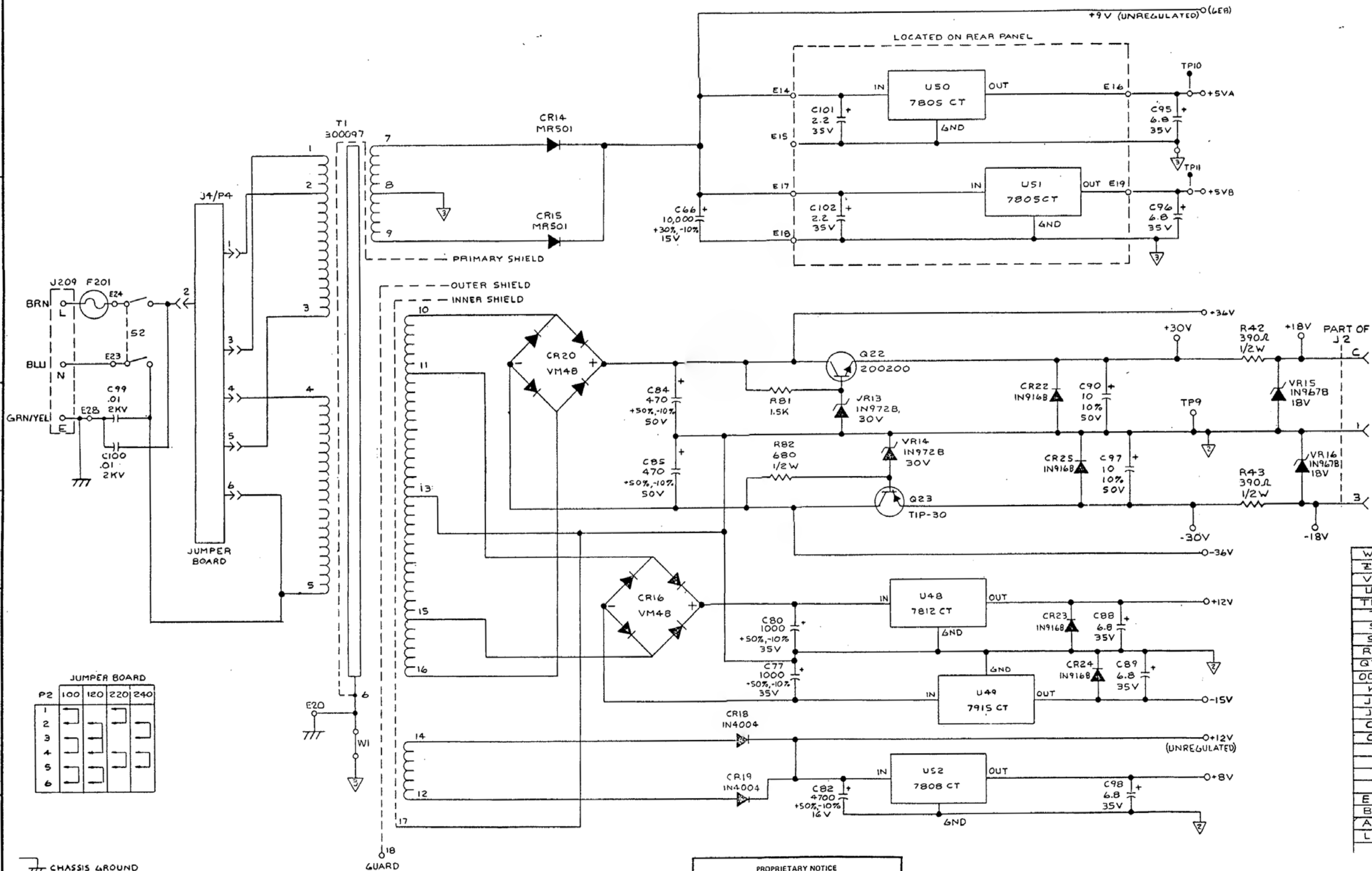
NOTES: UNLESS OTHERWISE SPECIFIED



PROPRIETARY NOTICE

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	401659	T
SCALE 2/1		SHEET 2 OF 15	

NOTES: UNLESS OTHERWISE SPECIFIED



JUMPER BOARD

P2	100	120	220	240
1				
2				
3				
4				
5				
6				

CHASSIS GROUND
DIGITAL GROUND
ANALOG COMMON
REFERENCE COMMON (MECCA)

3. RESISTOR NETWORKS ± 2%.
2. CAPACITORS ARE IN MF, ± 20%, 100V
1. RESISTORS ARE IN OHMS, ± 5%, 1/4 W

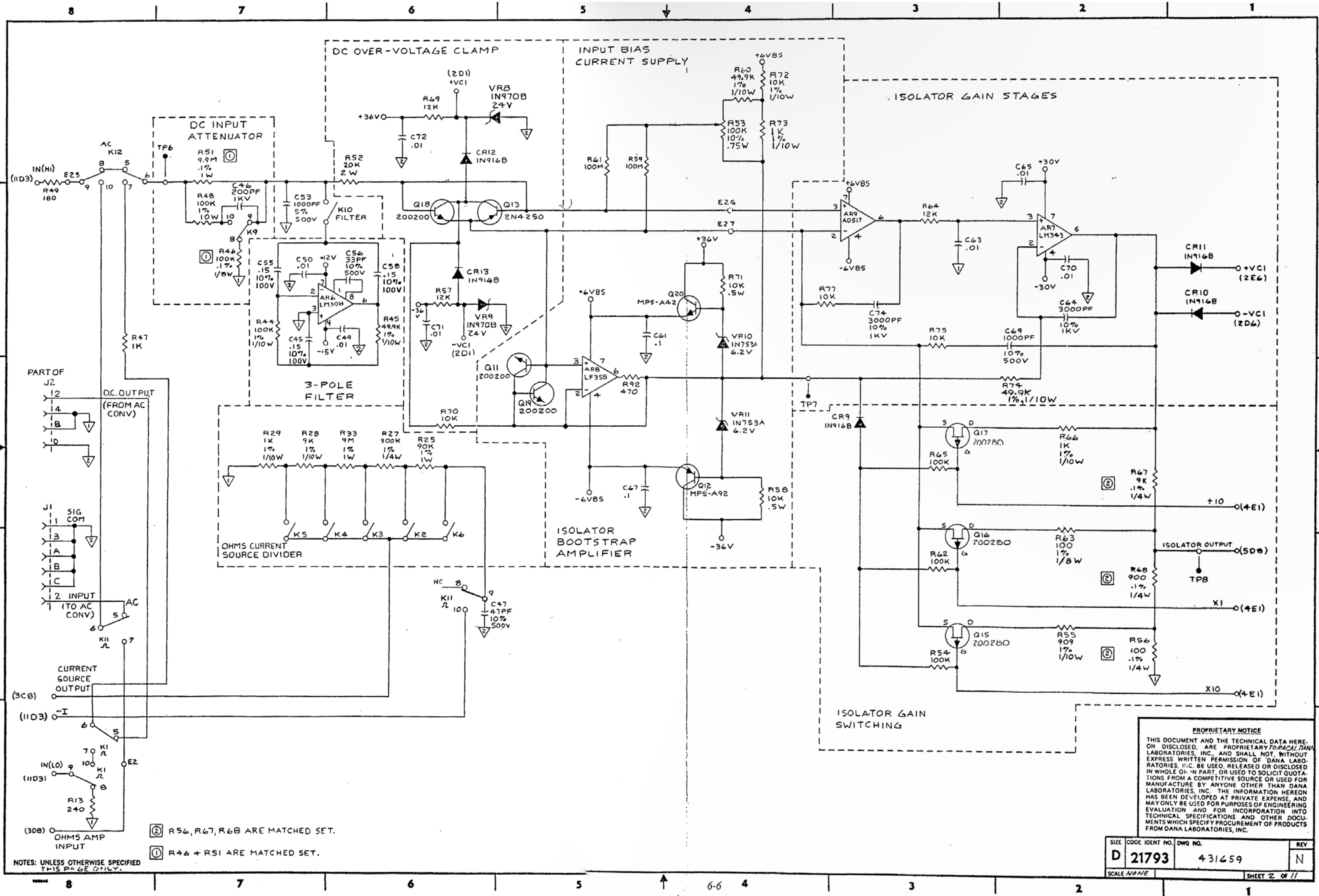
NOTES: UNLESS OTHERWISE SPECIFIED FOR PAGES 1-11.

W3	W2
Z10	
VR16	
U53	U4,29,30
TP11	
T1	
S201	
S2	
R96	R12,36,78,83-90
Q23	Q14
OCI 3	
K13	
J201	
J4/P4	
CR26	CR 3, 4, 7, 8,
C108	C2, 8, 9, 12, 13, 23, 28, 25
	32, 33, 34, 35, 36, 37, 40,
	41, 42, 43, 44, 48, 51, 57,
	78, 83, 86, 87, 91, 92, 93,
	94, 104, 105,
E28	
BT 1	
AR 9	AR4
LAST	NOT USED DESIGNATORS

SCHEMATIC-
MOTHERBOARD

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	431659	N

SCALE NONE SHEET 1 OF 11



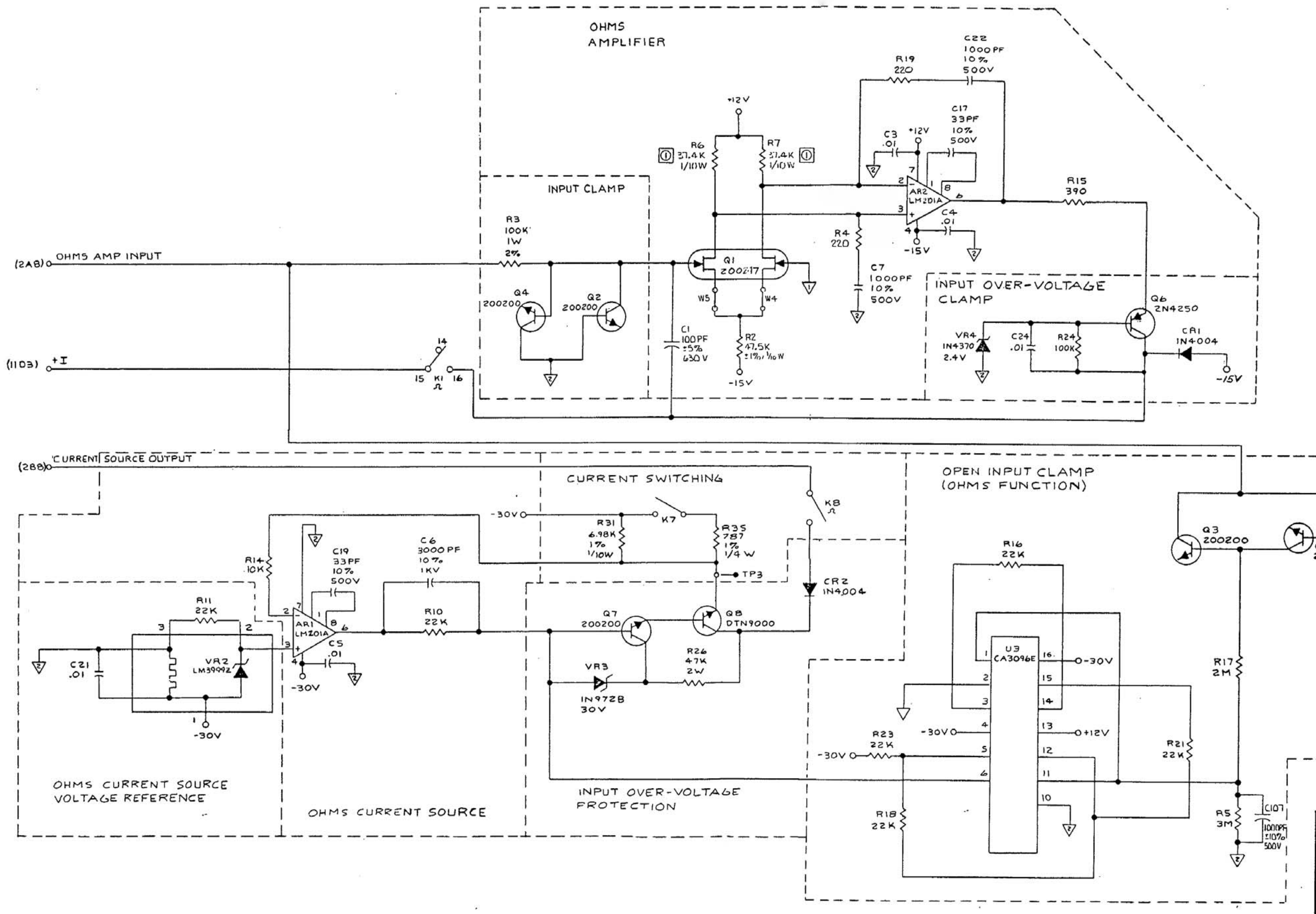
② R56, R67, R68 ARE MATCHED SET.

① R46 + R51 ARE MATCHED SET.

NOTES: UNLESS OTHERWISE SPECIFIED THIS PAGE ONLY.

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	431659	N

SCALE NONE — SHEET 2 OF 11

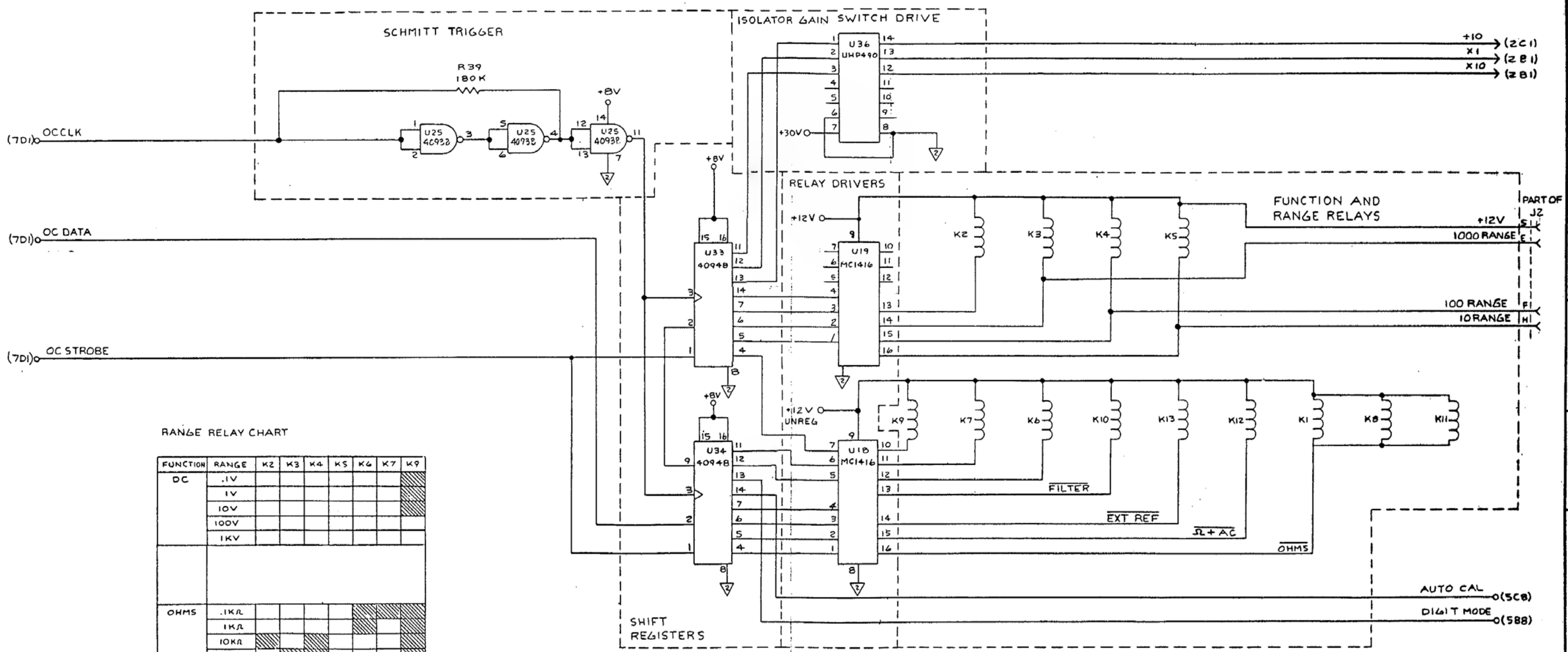


Ⓘ RESISTORS R6 & R7 ARE A MATCHED PAIR.

NOTES: UNLESS OTHERWISE SPECIFIED

PROPRIETARY NOTICE

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	431659	N
SCALE NONE		SHEET 3 OF 11	



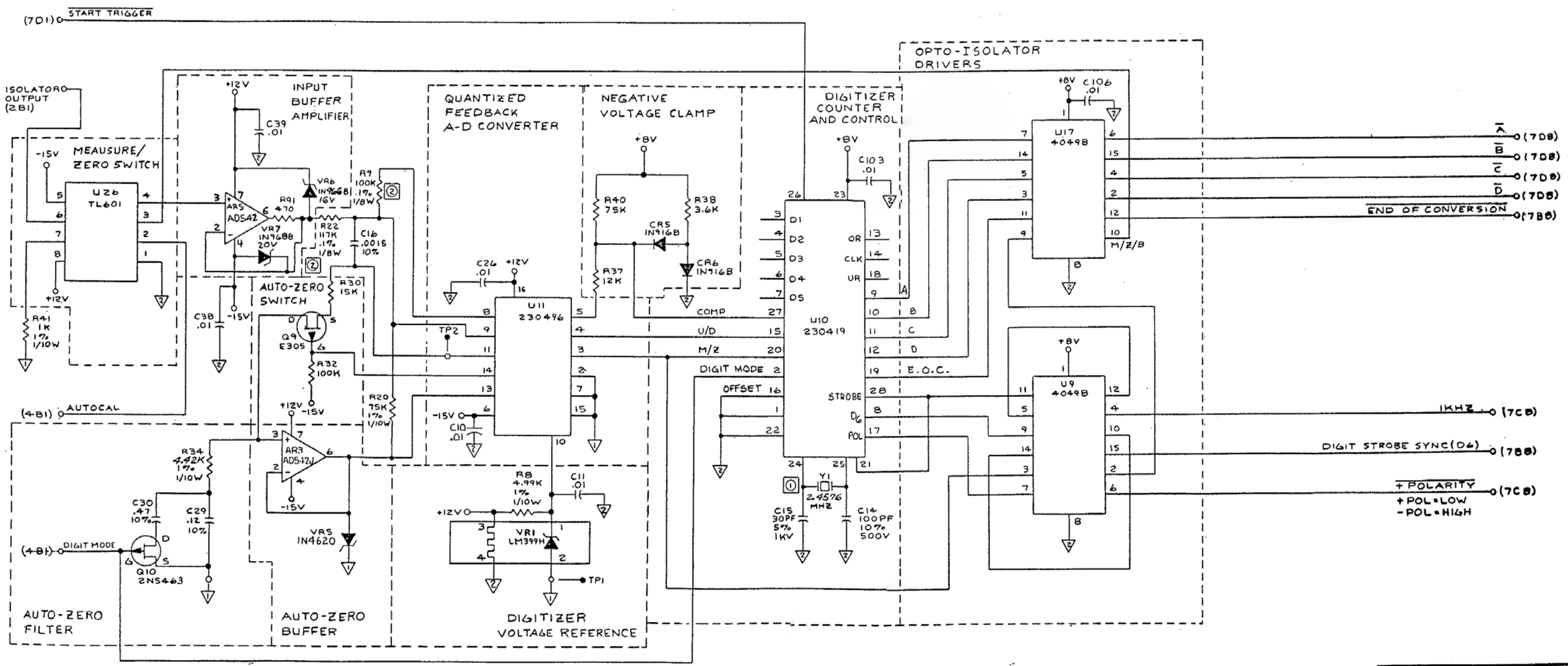
RANGE RELAY CHART

FUNCTION	RANGE	K2	K3	K4	K5	K6	K7	K9
DC	.1V							▨
	1V							▨
	10V							▨
	100V							
	1KV							
OHMS	.1KΩ					▨	▨	▨
	1KΩ					▨		▨
	10KΩ	▨		▨				▨
	100KΩ		▨	▨				▨
	1000KΩ			▨				▨
	10,000KΩ				▨			▨

▨ ENERGIZED

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	431659	N
SCALE NONE		SHEET 4 OF 11	

NOTES: UNLESS OTHERWISE SPECIFIED

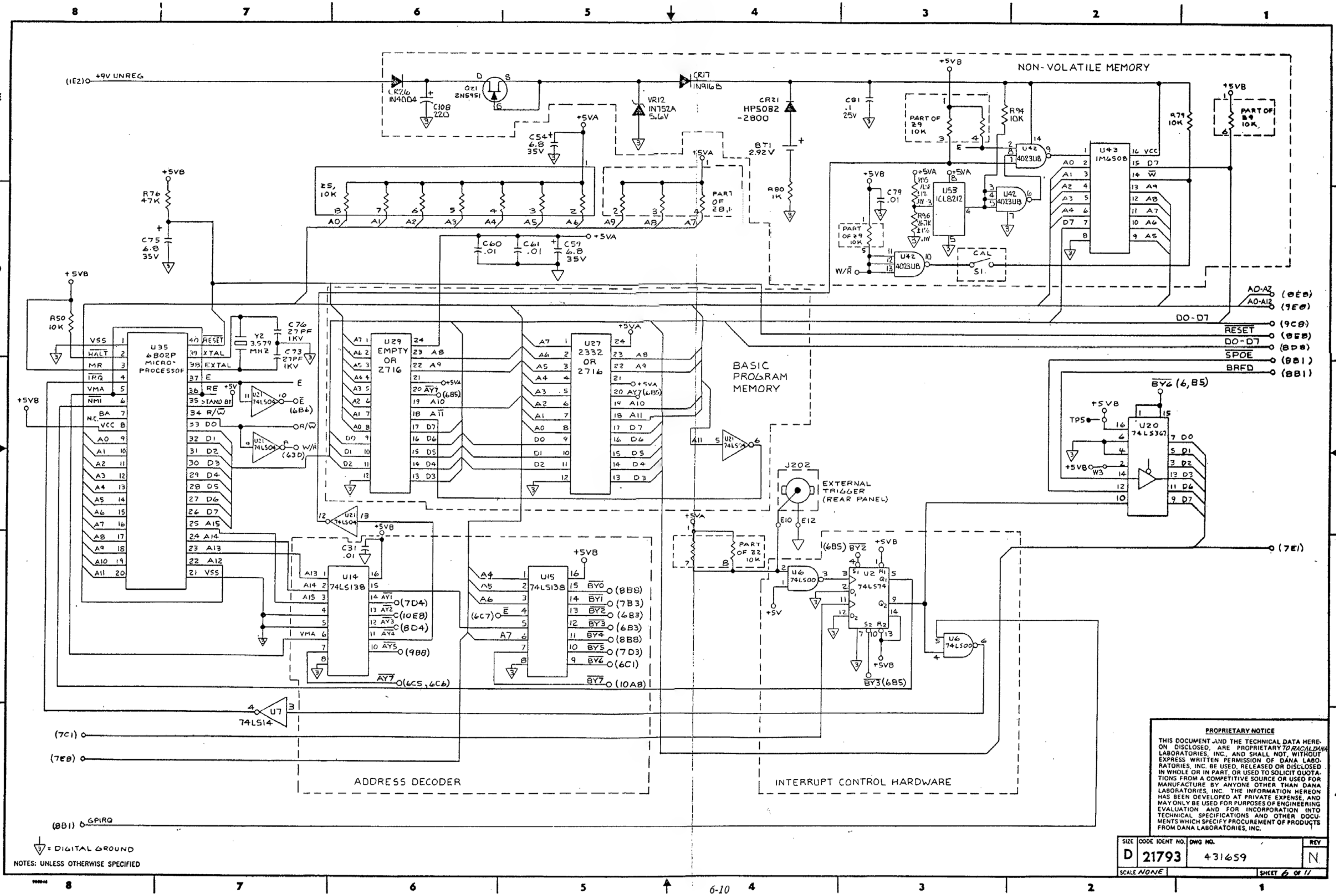


② R9 AND R22 IS MATCHED RESISTOR SET.

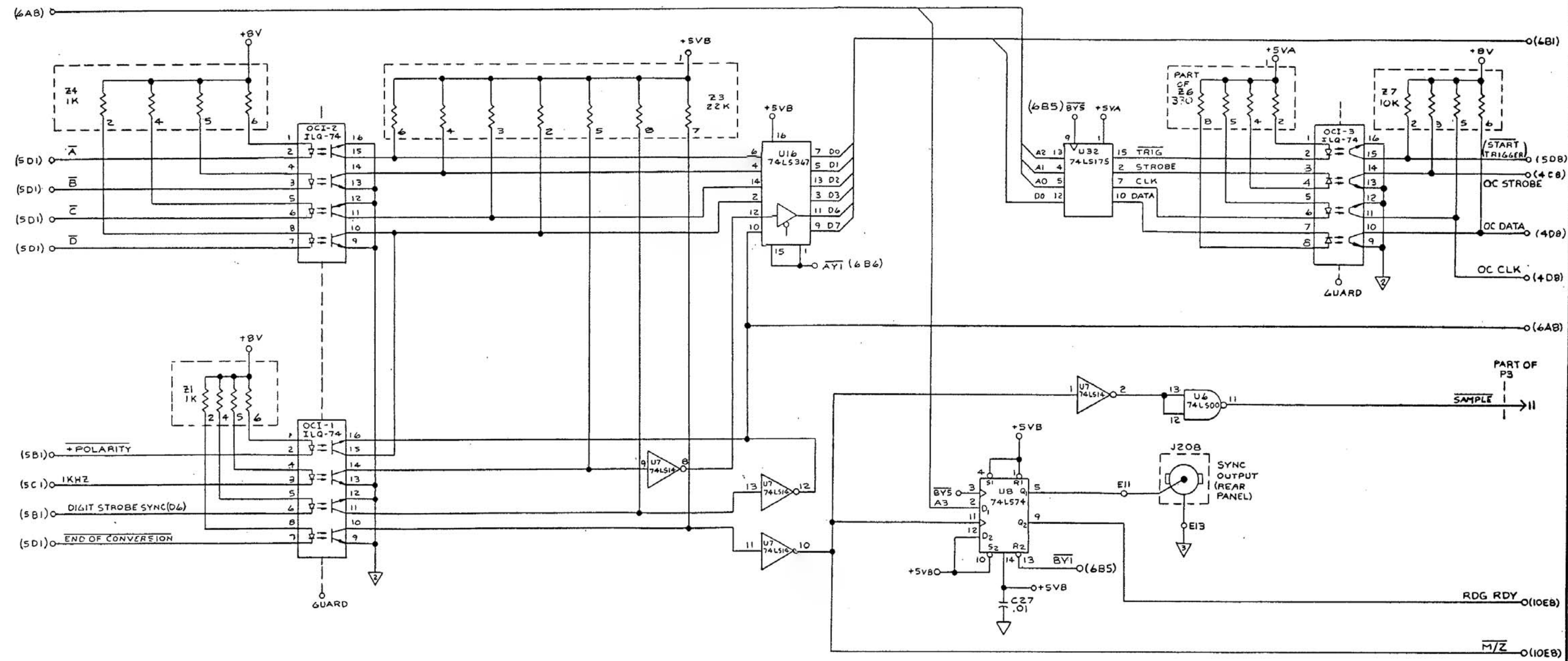
① 2.4576 MHZ FOR 60HZ.
2.048 MHZ FOR 50HZ.

NOTES: UNLESS OTHERWISE SPECIFIED THIS PAGE ONLY.

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	431659	N
SCALE NONE		SHEET 5 OF 11	



SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	431659	N
SCALE NONE			SHEET 6 OF 11



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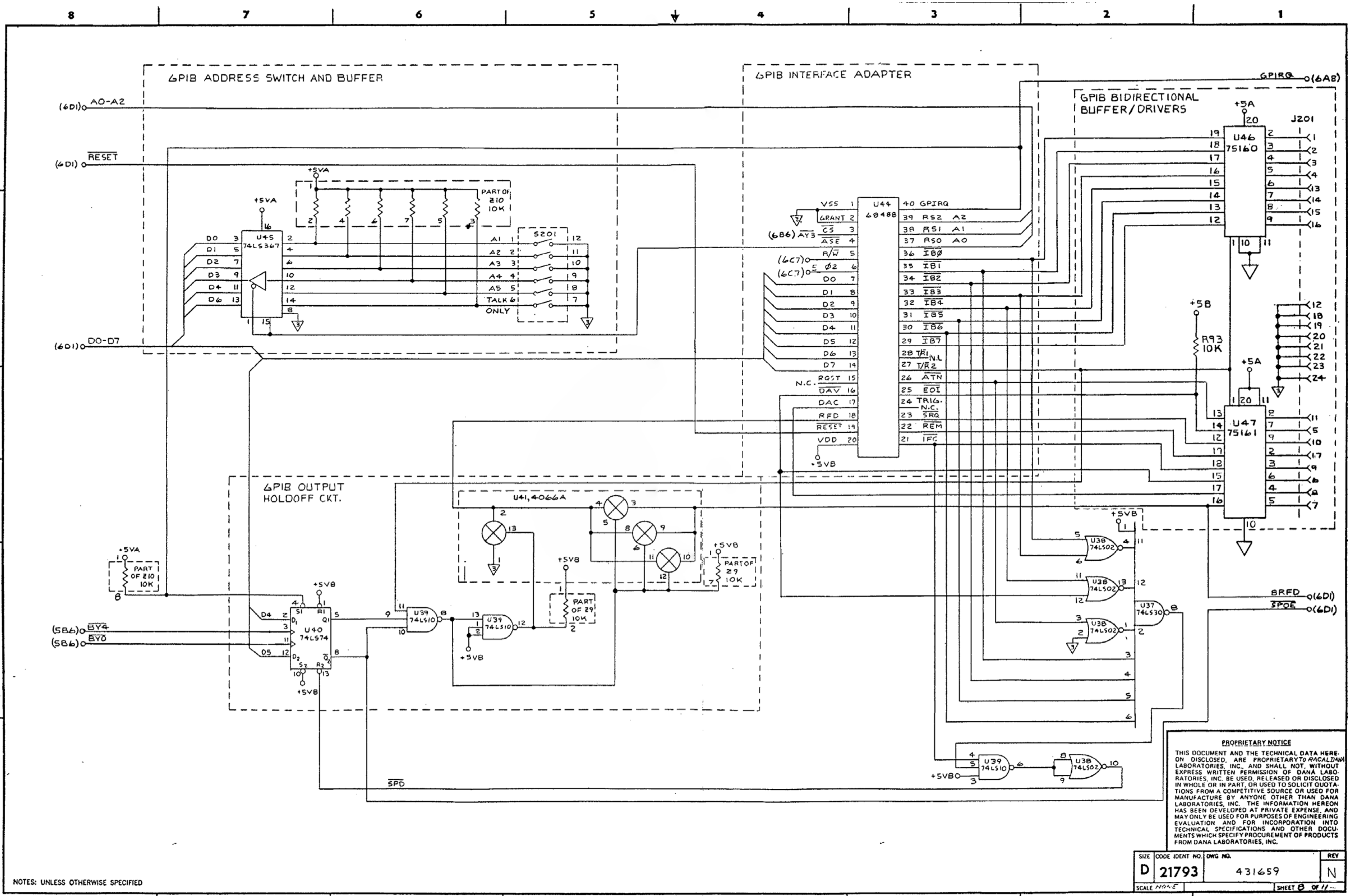
SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	431659	N
SCALE NONE		SHEET 7 OF 11	

NOTES: UNLESS OTHERWISE SPECIFIED



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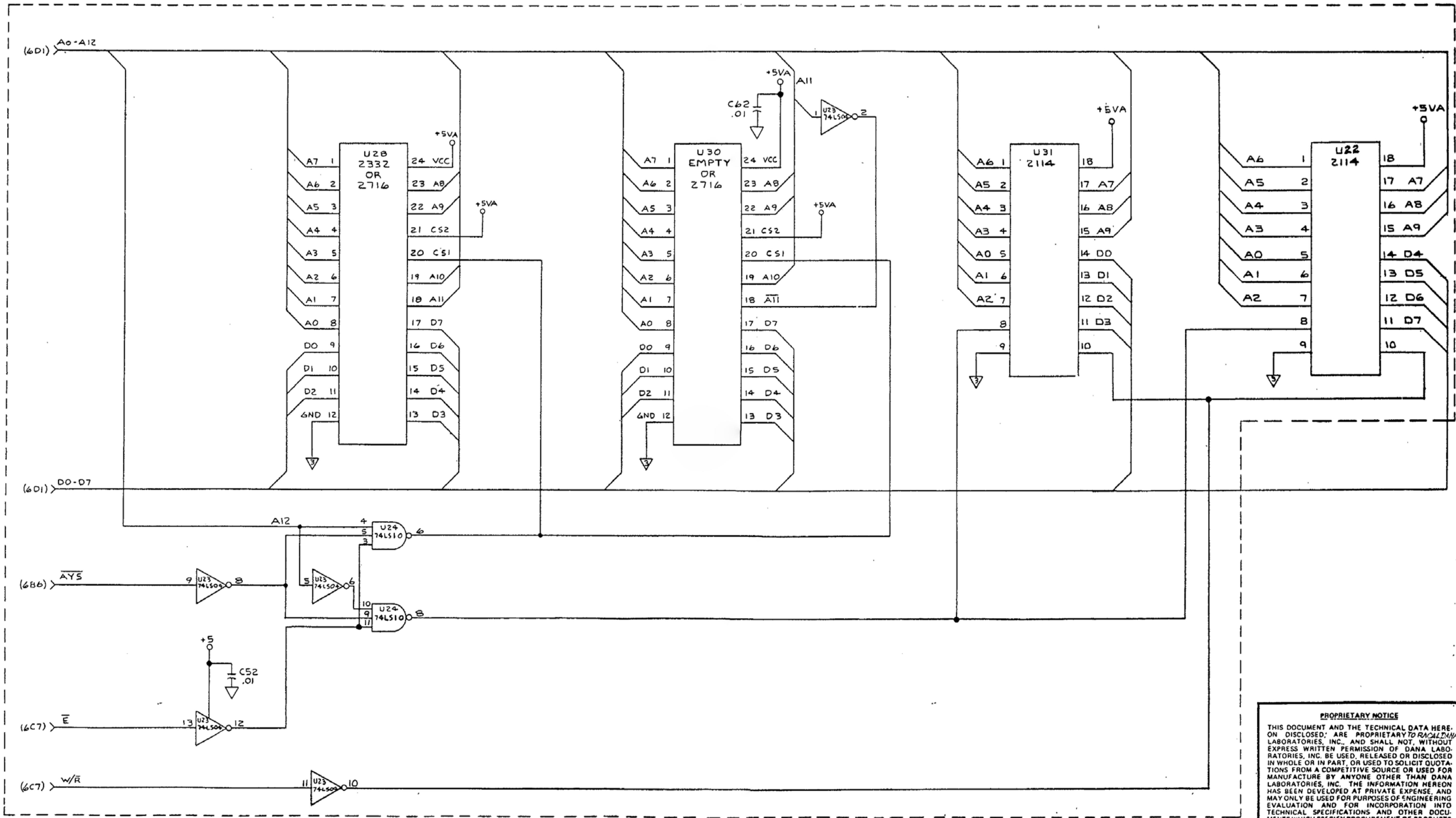
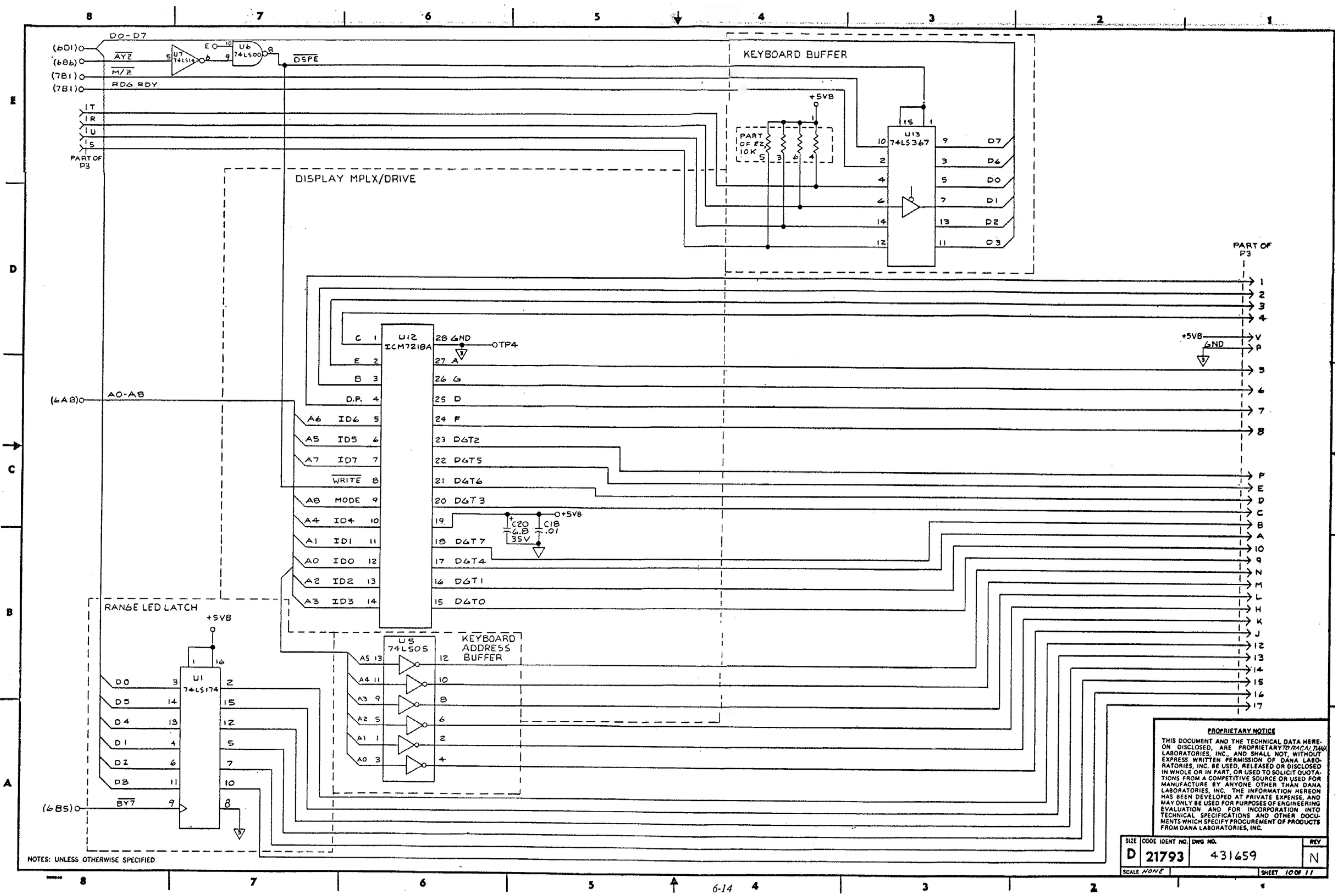
SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	431659	N
SCALE NONE			SHEET 8 OF 11



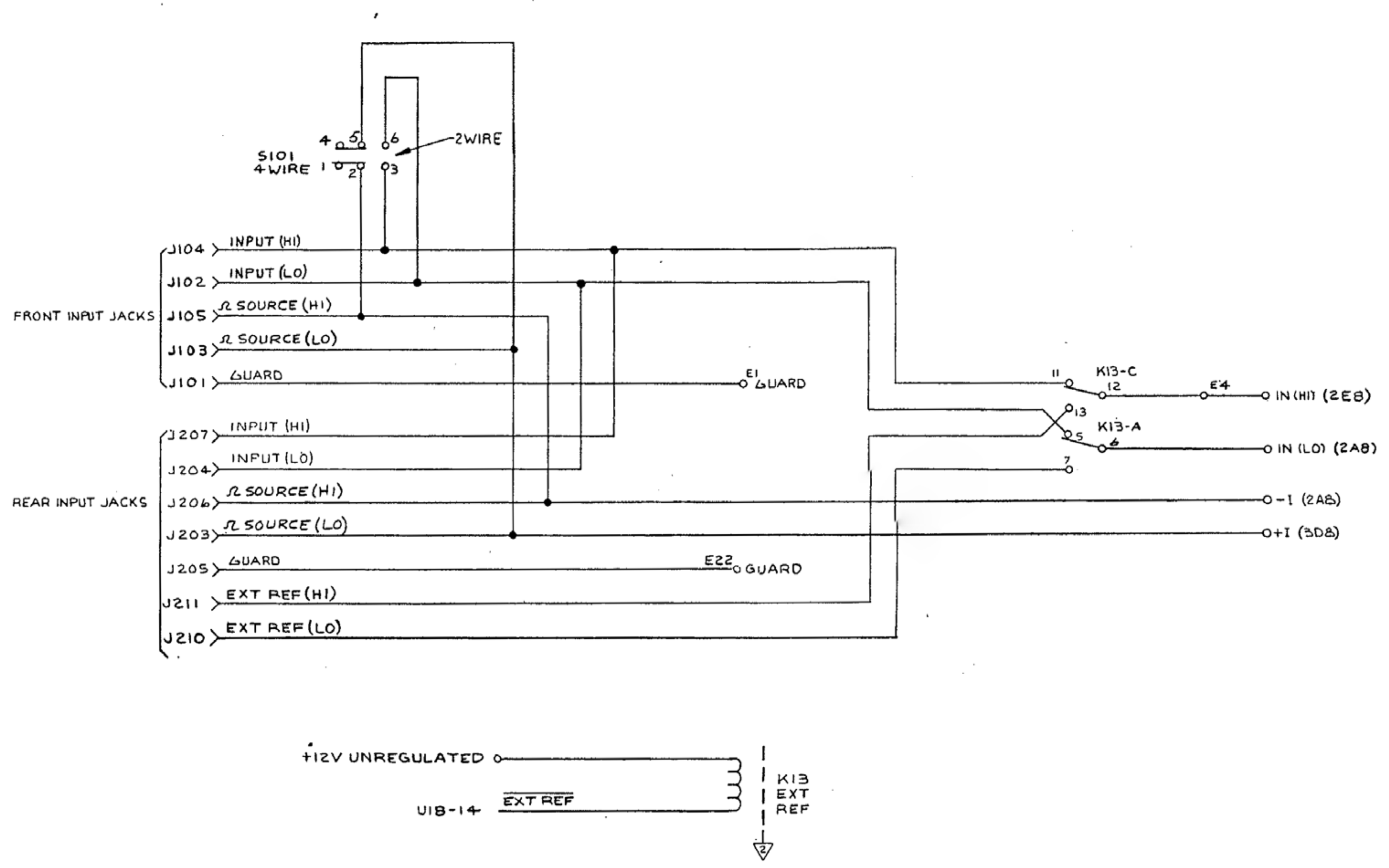
NOTES: UNLESS OTHERWISE SPECIFIED

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	431659	N
SCALE NONE		SHEET 9 OF 11	



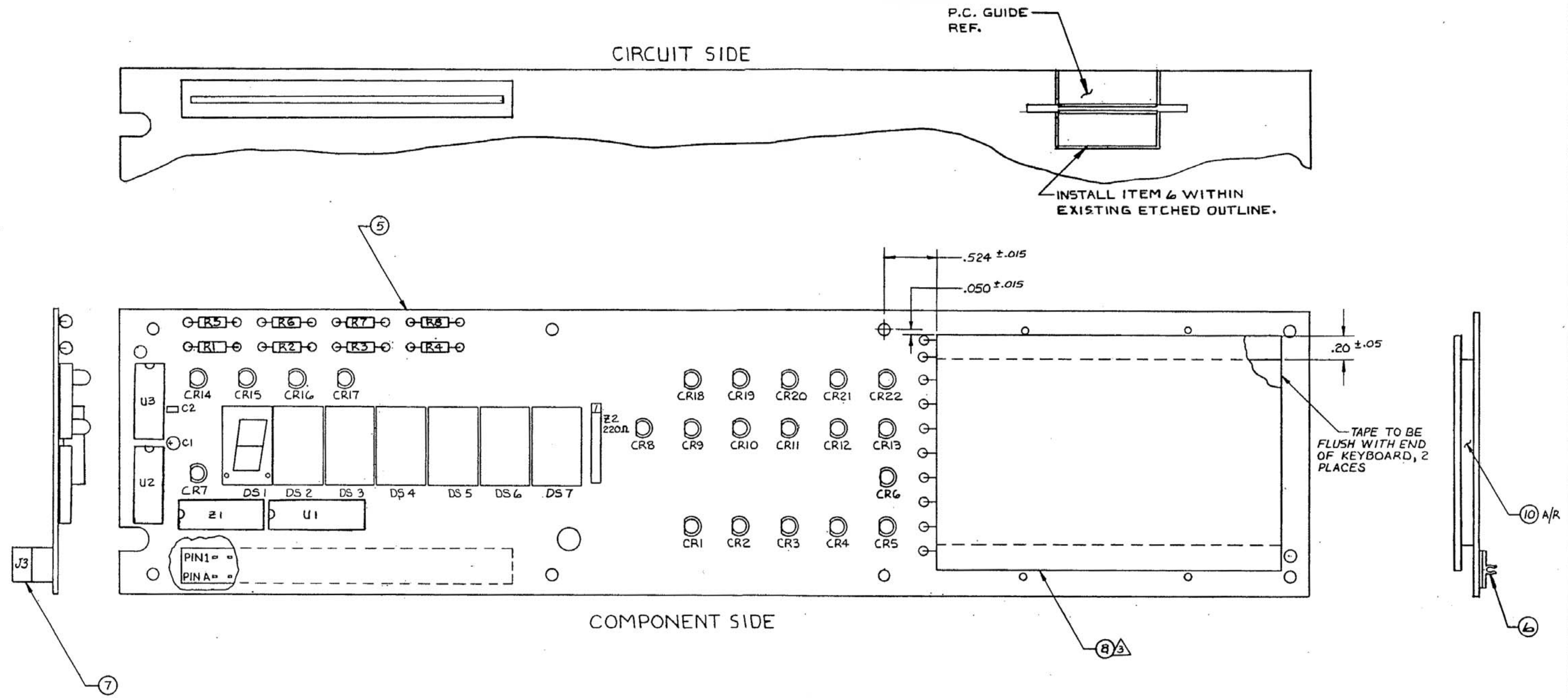
SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	431659	N

SCALE NONE | SHEET 10 OF 11



NOTES: UNLESS OTHERWISE SPECIFIED

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	431659	N
SCALE NONE		SHEET 11 OF 11	



4. ALL RESISTORS ARE 1/4W, 5%, 4.3Ω.

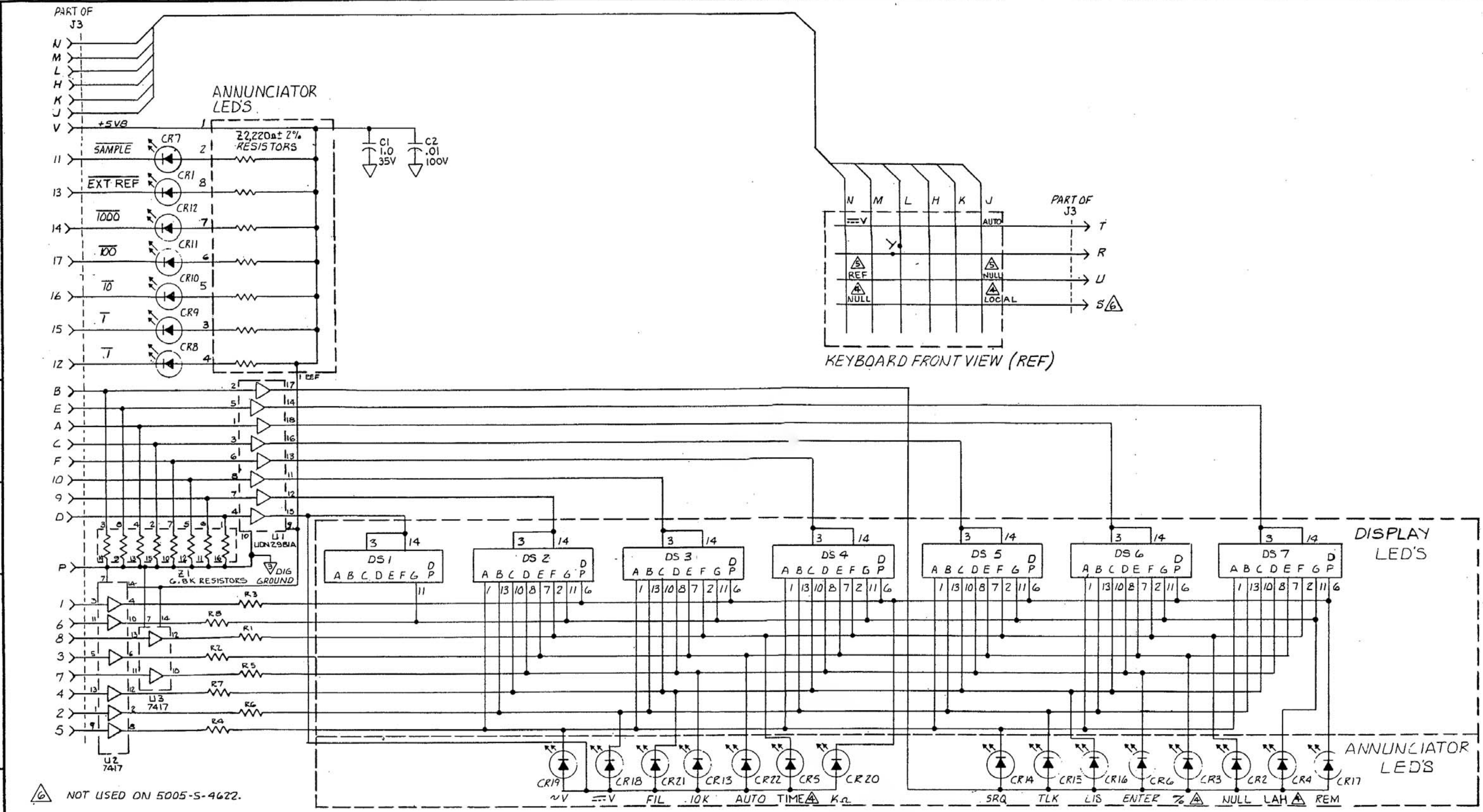
3. INSTALL USING ASSEMBLY TOOL 990097.

2. SCHEMATIC REFERENCE 431651.

1. ASSEMBLE PER RACAL-DANA WORKMANSHIP STANDARDS.

NOTES: UNLESS OTHERWISE SPECIFIED

P.C.B. ASSY, DISPLAY			
SIZE D	CODE IDENT NO. 21793	DWG NO. 401651	REV C
SCALE 2/1			SHEET 1 OF 2



6. NOT USED ON 5005-S-4622.

5. 5005-S-4622 ONLY.

4. 5005 ONLY.

3. CR1 THRU CR22 ARE 210072.

2. DS1 THRU DS7 ARE 210074.

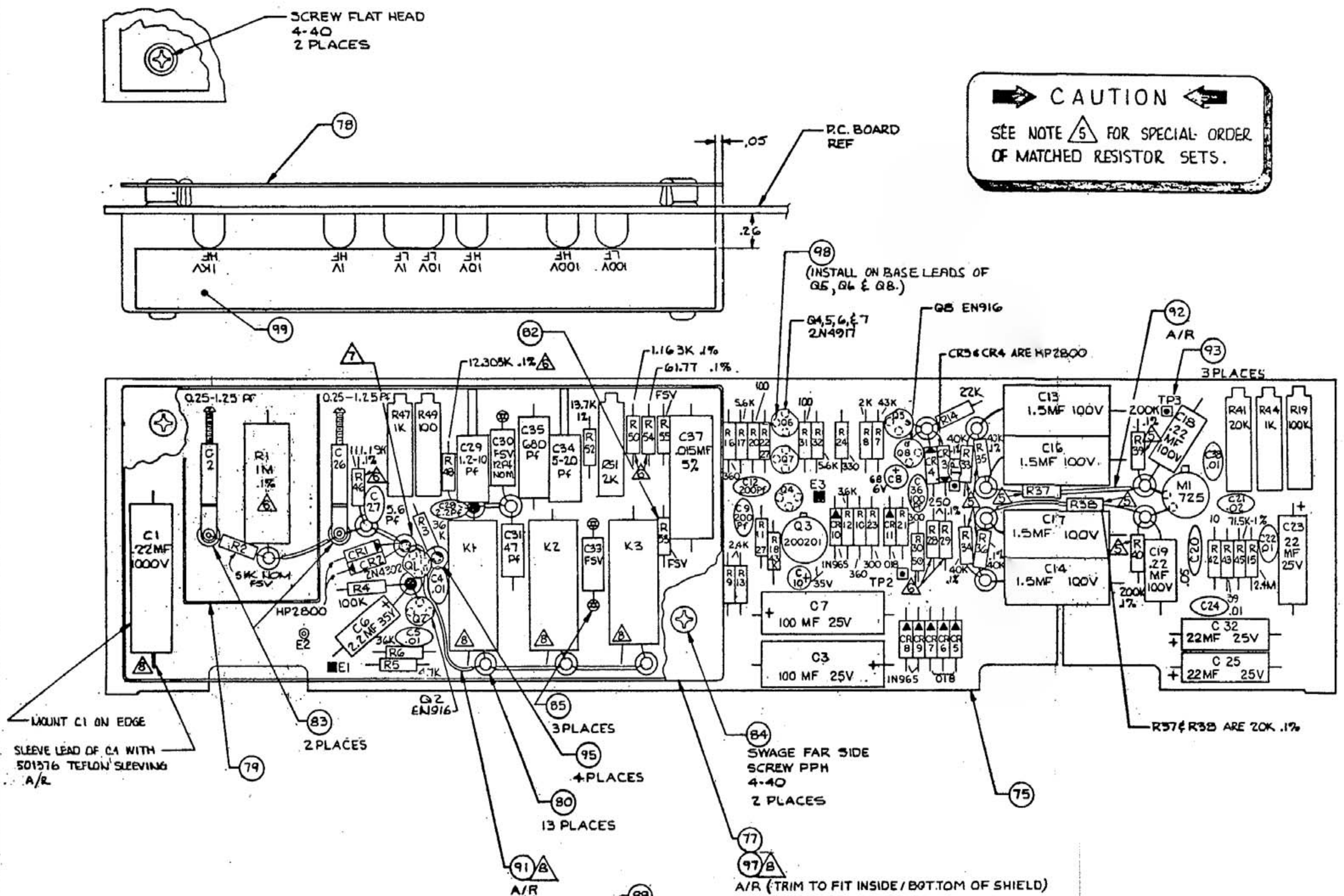
1. R1-R8 ARE 1/4W, 5%, 4.3Ω

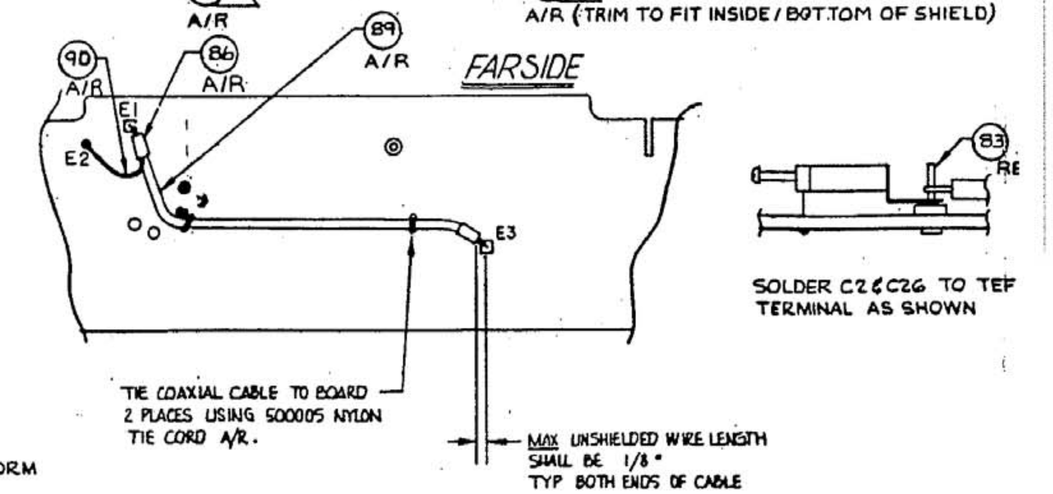
NOTES: UNLESS OTHERWISE SPECIFIED

SCHEMATIC, DISPLAY

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	431651	C

SCALE NONE · SHEET 1 OF 1



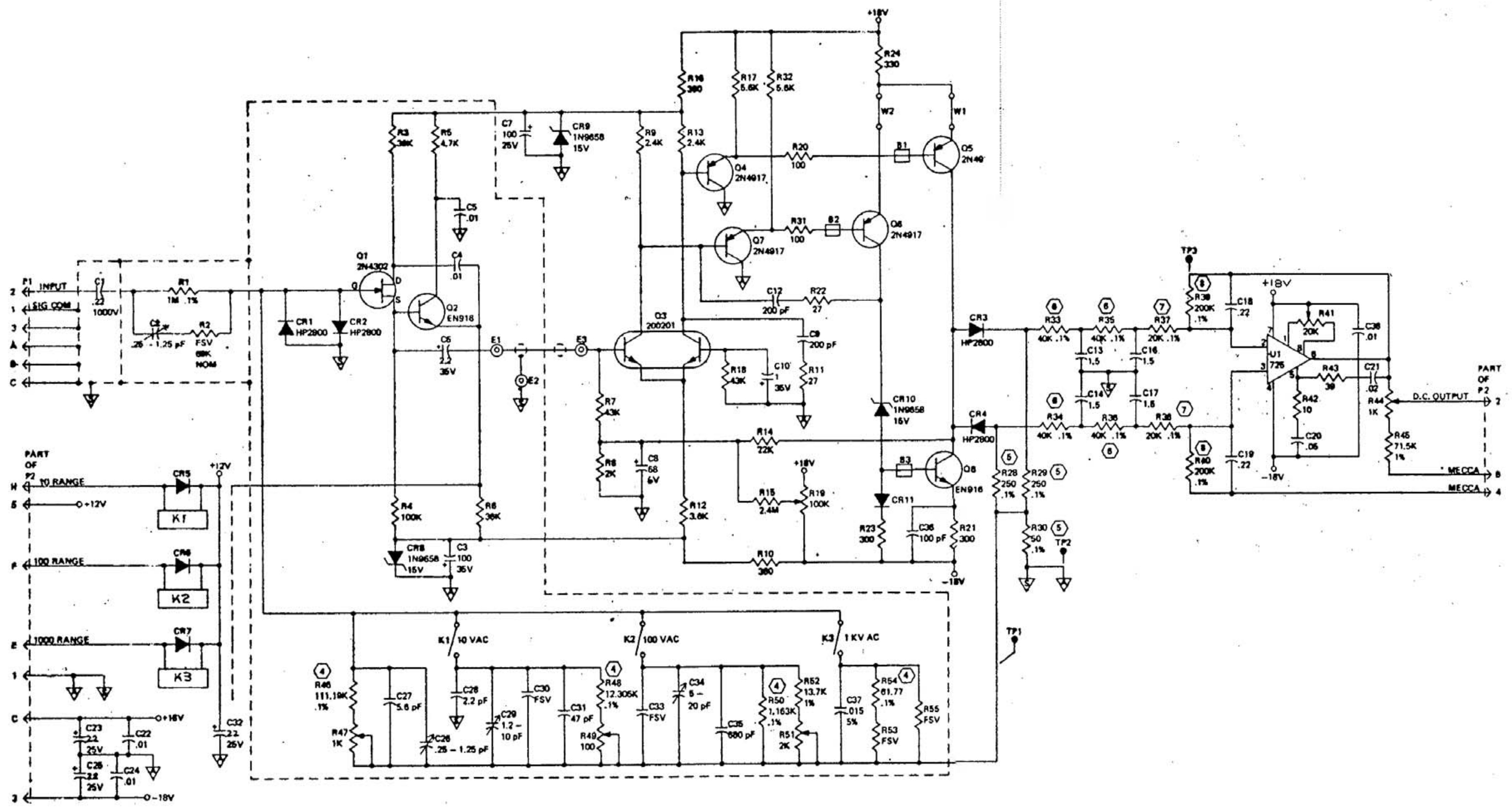


8. TAKE SPECIAL CARE TO DRESS LEADS OF K1, K2, K3, C1, & HARD WIRES SO THEY DO NOT INTERFERE WITH 453721 SHIELD.
7. USE HEATSINK CLIPS ON Q1 WHILE SOLDERING.
6. MATCHED RESISTOR SETS
   R28, R29, R30 MATCHED SET OF 3
   R1, R46, R48, R50, R54 MATCHED SET OF 5.
5. MATCHED RESISTOR SETS OF 2
   R37 & R38 MATCHED PAIR
   R33 & R34
   R35 & R36
   R39 & R40 MATCHED PAIR
4. ALL CAPACITORS ARE IN MFD.
3. REF SCHEMATIC NO. 432131
2. ALL RESISTORS ARE IN OHMS 1/4W, ±5%.
1. ASSY PROCESSES & PROCEDURES TO CONFORM TO DANA WORKMANSHIP STANDARDS.

NOTES: UNLESS OTHERWISE SPECIFIED

P.C.B. ASSY, AC CONVERTER

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	404107	A
SCALE 2/1		SHEET 1 OF 7	

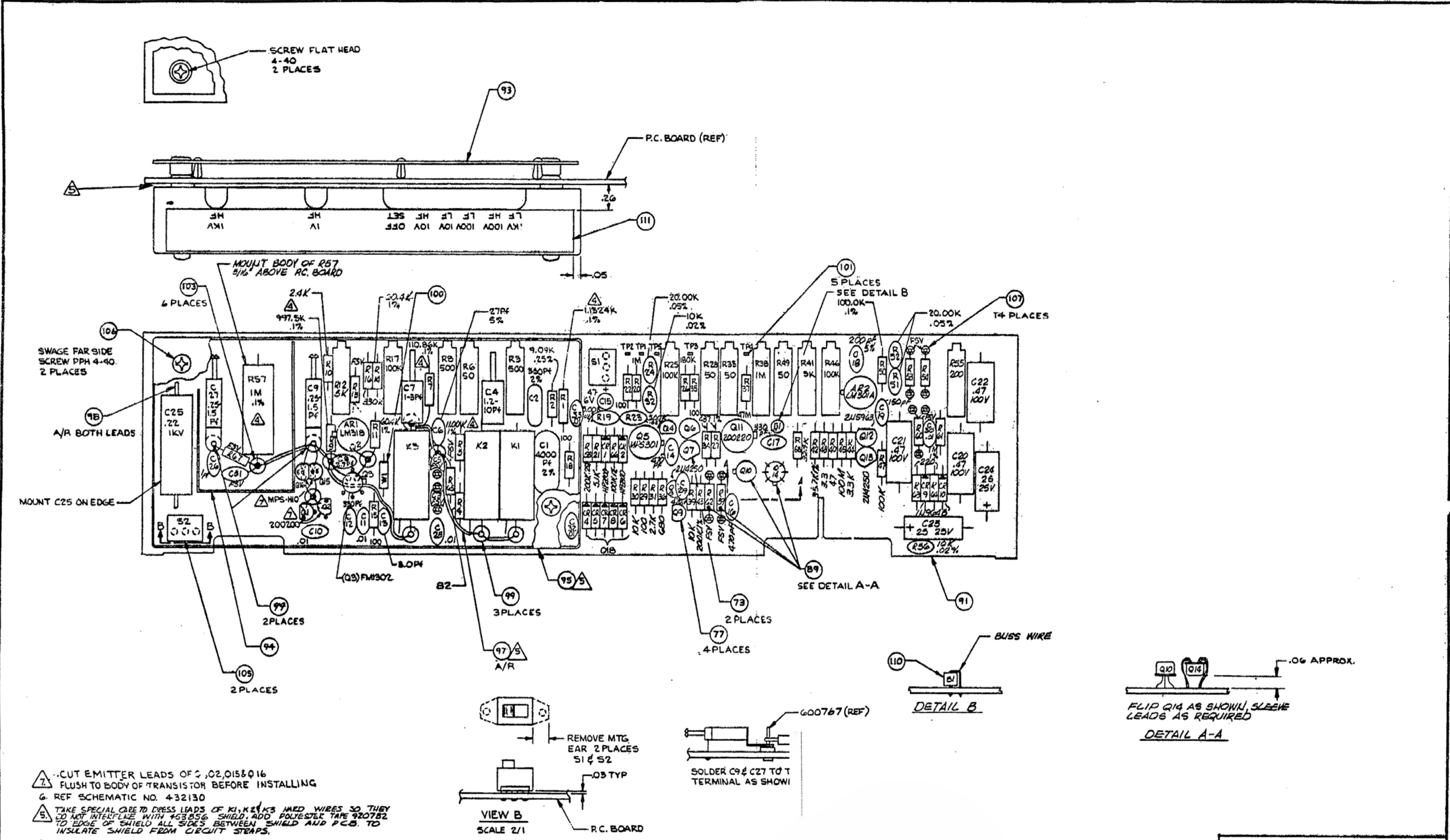


9. ASSY 404107
8. R39 AND R40 ARE RESISTOR SET 010792
7. R37 AND R38 ARE RESISTOR SET 010743
6. R33, R34, AND R36 ARE RESISTOR SET 010744
5. R28, R29, AND R30 ARE RESISTOR SET 010793
4. R46, R48, R50, AND R54 ARE RESISTOR SET 010794
3. DIODES ARE 018
2. CAPACITORS ARE IN μF
1. RESISTORS ARE IN OHMS, ±5%, 1/4W

NOTES: UNLESS OTHERWISE SPECIFIED

SCHEMATIC —
AC CONVERTER

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	432131	A
SCALE		SHEET 1 OF 1	



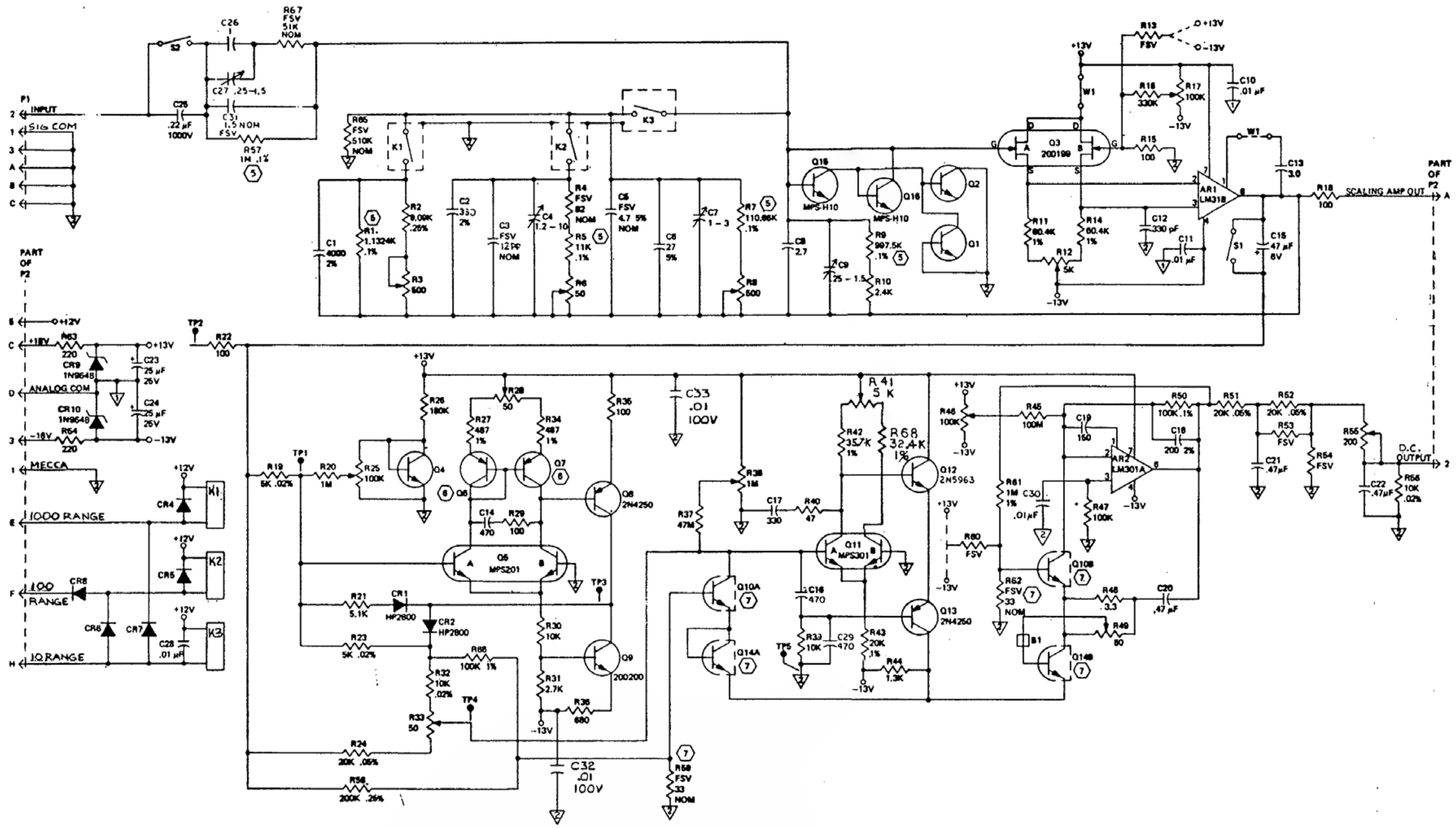
7. CUT EMITTER LEADS OF Q1, Q2, Q15 & Q16 FLUSH TO BODY OF TRANSISTOR BEFORE INSTALLING
6. REF SCHEMATIC NO. 432130
5. TAKE SPECIAL CARE TO DRESS LEADS OF K1, K2 & K3 AND WIRES SO THEY DO NOT INTERFERE WITH 463856 SHIELD. ADD POLYESTER TAPE 920782 TO EDGE OF SHIELD ALL SIDES BETWEEN SHIELD AND PCB. TO INSULATE SHIELD FROM CIRCUIT STRAPS.
4. MATCHED RESISTOR SET OF 5 R1, R5, R7, R9, R57
3. ALL CAPACITORS ARE IN MFD. 100V.
2. ALL RESISTORS ARE IN OHMS 1/4W, ±5%.
1. ASSY PROCESSES & PROCEDURES TO CONFORM TO DANA WORKMANSHIP STANDARDS.

NOTES: UNLESS OTHERWISE SPECIFIED

PCB ASSY
RMS CONVERTER

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	404106	E

SCALE 2/1 SHEET 1 OF 7



8 ASSY 404106

7. Q10 & Q14, R59 & R62 ARE LOG TRANSISTOR KIT 403865

6. Q6 & Q7 ARE MATCHED PAIR 200112

5. R1, R5, R7, R9 & R57 ARE RESISTOR SET 010721

4 TRANSISTORS ARE 200200

3. DIODES ARE 018

2. CAPACITORS ARE IN pF

1. RESISTORS ARE IN OHMS, ±5%, 1/4W

NOTES UNLESS OTHERWISE SPECIFIED

SCHEMATIC – RMS CONVERTER

SIZE	CODE IDENT NO.	DWG NO.	REV
D	21793	432130	A
SCALE		SHEET 1 OF 1	

SECTION 7 PARTS LIST

7.1 This section contains lists of replaceable parts arranged in the order of the following subassemblies:

7.2 Manufacturers are identified by FSC numbers listed in Table 7.1, "List of Suppliers". The code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1, H4-2, and their supplements.

Table 7.1 - List of Suppliers

FSC	NAME
00779	AMP, INC. HARRISBURG, PENNSYLVANIA
01121	ALLEN BRADLEY CO. MILWAUKEE, WISCONSIN
01281	TRW SEMICONDUCTORS LAWNDALE, CALIFORNIA
01295	TEXAS INSTRUMENTS, INC. DALLAS, TEXAS
02114	FERROXCUBE CORP. SAUGERTIES, NEW YORK
02660	AMPHENOL CORP. BROADVIEW, ILLINOIS
02735	RCA SOLID STATE DIV. SOMERVILLE, NEW JERSEY
03888	PYROFILM CORP. WHIPPANY, NEW JERSEY
04222	AEROVOX CORP. (HI-Q DIV.) MYRTLE BEACH, SOUTH CAROLINA
04713	MOTOROLA, INC. (SEMI-CONDUCTOR PRODUCTS DIV.) PHOENIX, ARIZONA
05276	POMONA ELECTRONICS CO., INC. POMONA, CALIFORNIA
05397	UNION CARBIDE CORP. (MATERIALS SYSTEMS DIV.) CLEVELAND, OHIO
06665	PRECISION MONOLITHICS SANTA CLARA, CALIFORNIA
07263	FAIRCHILD (SEMICONDUCTOR DIV.) MOUNTAIN VIEW, CALIFORNIA
08257	NPC ELECTRONICS CANOGA PARK, CALIFORNIA
09023	CORNELL-DUBILIER ELECTRONICS SANFORD, NORTH CAROLINA
11236	CTS OF BERNE, INC. BERNE, INDIANA

FSC	NAME
11237	CTS KEENE, INC. PASO ROBLES, CALIFORNIA
14298	AMERICAN COMPONENTS, INC. CONSHOHOCKEN, PENNSYLVANIA
15636	ELEC-TROL, INC. SAUGUS, CALIFORNIA
18612	VISHAY RESISTOR PRODUCTS MALVERN, PENNSYLVANIA
21317	ELECTRONIC APPLICATIONS CO. SO. EL MONTE, CALIFORNIA
21551	C-F ELECTRONICS, INC. VAN NUYS, CALIFORNIA
21793	RACAL-DANA INSTRUMENTS INC. IRVINE, CALIFORNIA
22045	JORDAN ELECTRIC COMPANY VAN NUYS, CALIFORNIA
24355	ANALOG DEVICES NORWOOD, MASSACHUSETTS
26625	MIAL USA, INC. NUTLEY, NEW JERSEY
26806	AMERICAN ZETTLER, INC. COSTA MESA, CALIFORNIA
27014	NATIONAL SEMI-CONDUCTOR CORP. SANTA CLARA, CALIFORNIA
27264	MOLEX PRODUCTS CO. DOWNERS GROVE, ILLINOIS
27556	IMB ELECTRONIC PRODUCTS, INC. SANTA FE SPRINGS, CALIFORNIA
27777	VARO ELECTRAN DEVICES, INC. GARLAND, TEXAS
32293	INTERSIL, INC. CUPERTINO, CALIFORNIA
34553	AMPEREX/MEPCO-ELECTRA (COMPONENT DIV.) HAUPPAUGE, NEW YORK

Table 7.1 - List of Suppliers continued

FSC	NAME
50434	HEWLETT-PACKARD CO. (HPA DIV.) PALO ALTO, CALIFORNIA
50579	LITRONIX, INC. CUPERTINO, CALIFORNIA
50857	DIONICS, INC. WESTBURY, NEW YORK
52763	STETTNER-TRUSH CAZENOVIA, NEW YORK
56289	SPRAGUE ELECTRIC CO. N. ADAMS, MASSACHUSETTS
71471	AEROVOX CORP. (CINEMA PLANT) MONCKS CORNER, SOUTH CAROLINA
71590	CENTRALAB ELECTRONICS MILWAUKEE, WISCONSIN
71707	COTO-COIL CO., INC. PROVIDENCE, RHODE ISLAND
71785	TRW ELECTRONIC COMPONENTS (CINCH DIV.) ELK GROVE VILLAGE, ILLINOIS
72136	ELECTRO-MOTIVE MANUFACTURING CO.,INC. WILLIAMANTIC, CONNECTICUT
72982	ERIE TECHNOLOGICAL PRODUCTS, INC. ERIE, PENNSYLVANIA
73138	BECKMAN INSTRUMENTS, INC. FULLERTON, CALIFORNIA
73445	AMPEREX ELECTRONIC CORP. HICKSVILLE, L.I., NEW YORK
74970	E. F. JOHNSON CO. WASECA, MINNESOTA
75915	LITTELFUSE, INC. DES PLAINES, ILLINOIS
79727	C–W INDUSTRIES WARMINSTER, PENNSYLVANIA
80131	ELECTRONICS INDUSTRIES ASSOC. WASHINGTON, D.C.
81349	MILITARY SPECIFICATION
82389	SWITCHCRAFT, INC. CHICAGO, ILLINOIS
90201	MALLORY CAPACITOR CO. INDIANAPOLIS, INDIANA
91637	DALE ELECTRONICS, INC. COLUMBUS, NEBRASKA

404136 . 404200 – CHASSIS ASSEMBLY (Includes Front Panel & Rear Panel)

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
F201	920204	FUSE SLO .50 A (100V, 120V Operation)	75915	3AG1/2ASB
	920802	FUSE SLO .25 A (220V, 240V Operation)	75915	213.250
J101	600980	POST BINDING, BANANA JACK, BLACK	05276	2854-0
J102	600980	POST BINDING, BANANA JACK, BLACK	05276	2854-0
J103	600980	POST BINDING, BANANA JACK, BLACK	05276	2854-0
J104	600989	POST BINDING, BANANA JACK, WHITE	05276	2854-9
J105	600989	POST BINDING, BANANA JACK, WHITE	05276	2854-9
J201	600957	RECEPT 24 POS	00779	552791-1
J202	600808	CONN BNC	02660	31-010
J203	600980	POST BINDING, BANANA JACK, BLACK	05276	2854-0
J204	600980	POST BINDING, BANANA JACK, BLACK	05276	2854-0
J205	600980	POST BINDING, BANANA JACK, BLACK	05276	2854-0
J206	600989	POST BINDING, BANANA JACK, WHITE	05276	2854-9
J207	600989	POST BINDING, BANANA JACK, WHITE	05276	2854-9
J208	600808	CONN BNC	02660	31-010
J209	600619	CONN RECPTLE	82389	EAC-301
J210	600980	POST BINDING, BANANA JACK, BLACK	05276	2854-0
J211	600989	POST BINDING, BANANA JACK, WHITE	05276	2854-9
S101	600910	SWITCH, MINIATURE		GF-323-440/GF20-30/ G02-150
S201	600814	SWITCH 6 SPST	11237	206-6

401659 – Assy., PCB, MOTHERBOARD

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
AR1	230411	IC OP AMP LM201A-H	27014	LM201A-H
AR2	230411	IC OP AMP LM201A-H	27014	LM201A-H
AR3	230543	IC LINEAR	24355	542
AR5	230543	IC LINEAR	24355	542
AR6	230103	IC	27014	LM308
AR7	230415	IC HI VOLTAGE OP AMP	27014	LM343H
AR8	230331	IC	27014	LF355H
AR9	230470	IC OP AMP AD517KH	24355	AD517KH
BT1	920847	BATTERY 3 VOLT LITHIUM ORGANIC	90201	L032S
C1	120034	CAP POLY 100 PFD 630 V 5%	08257	KSO Series
C3	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C4	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C5	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C6	100043	CAP CERAM .003-PFD 1000 V 10%	71590	DD302
C7	101174	CAP CERAM .001 MFD 500 V 10%	04222	SCD-DI-2X5F-1000
C10	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C11	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C14	101145	CAP CERAM 100 PFD 500 V 10%	04222	TCD-DI-1N5600-100
C15	100099	CAP CERAM 30 PFD 1000 V 5%	56289	C030B102F300J
C16	121473	CAP MYLAR .0015 MFD 100 V 10%	09023	WMF1S47
C17	100012	CAP CERAM 33 PFD 500 V 10%	71471	TCD-DI-1(N750)
C18	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C19	100012	CAP CERAM 33 PFD 500 V 10%	71471	TCD-DI-1(N750)
C20	110126	CAP TANTA 6.8 MFD 35 V 20%	05397	T368B685M035AS
C21	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C22	101174	CAP CERAM .001 MFD 500 V 10%	04222	SCD-DI-2X5F-1000
C24	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C26	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C27	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C29	120352	CAP MYLAR .12 μF 100 V 10%	09023	WMF1P12
C30	120026	CAP MYLAR .47 MFD 100 V 10%	27556	SAZB474K
C31	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C38	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C39	100017	CAP CERAM .01 MFD 100 V 20%	56289	C023B101F103M
C45	120351	CAP POLY .15 μF 50 V 10%	09023	MCR1P15
C46	100040	CAP CERAM 200 PFD 1000 V 20%	56289	C023B102E201M
C47	101182	CAP CERAM 47 PFD 500 V 10%	71471	TCD-DI-2(N750)

REF DES	RACAL-DANA P/N	DESCRIPTION					FSC	MANU P/N
C49	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C50	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C52	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C53	120004	CAP	POLY	.001 MFD	500 V	5%	08257	KSO Series
C54	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C55	120351	CAP	POLY	.15 µF	50 V	10%	09023	MCR1P15
C56	100012	CAP	CERAM	33 PFD	500 V	10%	71471	TCD-DI-I(N750)
C58	120351	CAP	POLY	.15 µF	50 V	10%	09023	MCR1P15
C59	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C60	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C61	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C62	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C63	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C64	100043	CAP	CERAM	.003 PFD	1000 V	10%	71590	DD302
C65	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C66	110197	CAP	ELECT	10,000 µF	16 V			VP16VB10000MC
C67	100027	CAP	CERAM	.1 MFD	100 V	20%	72982	845-000-X5V01042
C68	100027	CAP	CERAM	.1 MFD	100 V	20%	72982	845-000-X5V01042
C69	101174	CAP	CERAM	.001 MFD	500 V	10%	04222	SCD-DI-2X5F-1000
C70	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C71	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C72	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C73	100016	CAP	CERAM	27 PFD	1000 V	10%	71590	DD270
C74	100043	CAP	CERAM	.003 PFD	1000 V	10%	71590	DD302
C75	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C76	100016	CAP	CERAM	27 PFD	1000 V	10%	71590	DD270
C77	110192	CAP	ELECT	1000 MFD	35 V			35TAL1000
C79	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C80	110192	CAP	ELECT	1000 MFD	35 V			35TAL1000
C81	100024	CAP	CERAM	.1 MFD	25 V		72982	5815-000Y5U104Z
C82	110185	CAP	ELECT	4700 MFD	16 V			16TAL4700
C84	110194	CAP	ELECT	470 MFD	50 V	Radial Lead		See Description
C85	110194	CAP	ELECT	470 MFD	50 V	Radial Lead		See Description
C88	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C89	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C90	110158	CAP	TANTA	10 MFD	50 V	10%	05397	T362C106K050A
C95	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C96	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C97	110158	CAP	TANTA	10 MFD	50 V	10%	05397	T362C106K050A
C98	110126	CAP	TANTA	6.8 MFD	35 V	20%	05397	T368B685M035AS
C99	100111	CAP	CERAM	.01 MFD	2000 V		71471	HVD6-2KV

401659 – Assy., PCB, MOTHERBOARD continued

REF DES	RACAL-DANA P/N	DESCRIPTION					FSC	MANU P/N
C100	100111	CAP	CERAM	.01 MFD	2000 V		71471	HVD6-2KV
C101	110125	CAP	TANTA	2.2 MFD	35 V	20%	05397	T368B225M035AS
C102	110125	CAP	TANTA	2.2 MFD	35 V	20%	05397	T368B225M035AS
C103	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C106	100017	CAP	CERAM	.01 MFD	100 V	20%	56289	C023B101F103M
C107	101174	CAP	CERAM	.001 MFD	500 V	10%	04222	SCD-DI-2X5F-1000
C108	110183	CAP	ELECT	200 MFD	16 V		34533	ET221X106A6
CR1	210004	DIODE	SILICO				81349	1N4004
CR2	210004	DIODE	SILICO				81349	1N4004
CR5	211083	DIODE	SILICO		1N916B		81349	1N916B
CR6	211083	DIODE	SILICO		1N916B		81349	1N916B
CR9	211083	DIODE	SILICO		1N916B		81349	1N916B
CR10	211083	DIODE	SILICO		1N916B		81349	1N916B
CR11	211083	DIODE	SILICO		1N916B		81349	1N916B
CR12	211083	DIODE	SILICO		1N916B		81349	1N916B
CR13	211083	DIODE	SILICO		1N916B		81349	1N916B
CR14	210070	DIODE	POWER	3 AMP			04713	MR501
CR15	210070	DIODE	POWER	3 AMP			04713	MR501
CR16	230465	IC	DIODE BRIDGE		VM48		27777	VM48
CR17	211083	DIODE	SILICO		1N916B		81349	1N916B
CR18	210004	DIODE	SILICO				81349	1N4004
CR19	210004	DIODE	SILICO				81349	1N4004
CR20	230465	IC	DIODE BRIDGE		VM48		27777	VM48
CR21	210015	DIODE					50434	HP5082-2800
CR22	211083	DIODE	SILICO		1N916B		81349	1N916B
CR23	211083	DIODE	SILICO		1N916B		81349	1N916B
CR24	211083	DIODE	SILICO		1N916B		81349	1N916B
CR25	211083	DIODE	SILICO		1N916B		81349	1N916B
CR26	210004	DIODE	SILICO				81349	1N4004
J1	600689	CONN	3 P				00779	4-583486-8
J2	600690	CONN	7 P				00779	4-583486-4
J4	600821	CONN	6 P				27264	09-03-1062
J201	600957	RECEPT		24 POS			00779	552791-1
K1	310146	RELAY	CRADLE	4 FORM C			26806	AZ421-08-204
K2	310145	RELAY	REED	1 FORM A			71707	CR-4573
K3	310145	RELAY	REED	1 FORM A			71707	CR-4573
K4	310145	RELAY	REED	1 FORM A			71707	CR-4573
K5	310145	RELAY	REED	1 FORM A			71707	CR-4573
K6	310145	RELAY	REED	1 FORM A			71707	CR-4573
K7	310145	RELAY	REED	1 FORM A			71707	CR-4573

401659 – Assy., PCB, MOTHERBOARD continued

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
K8	310145	RELAY REED 1 FORM A	71707	CR-4573
K9	310147	RELAY CRADLE 2 FORM C	26806	AZ420-08-205
K10	310144	RELAY REED 1 FORM A	21317	1A12R960DIAA
K11	310147	RELAY CRADLE 2 FORM C	26806	AZ420-08-205
K12	310147	RELAY CRADLE 2 FORM C	26806	AZ420-08-205
K13	310146	RELAY CRADLE 4 FORM C	26806	AZ421-08-204
OCI1	230456	IC QUAD OPTO-ISOLATOR	50579	ISO-L1TQ74
OCI2	230456	IC QUAD OPTO-ISOLATOR	50579	ISO-L1TQ74
OCI3	230456	IC QUAD OPTO-ISOLATOR	50579	ISO-L1TQ74
P4	410727	PCB ASSY LINE VOLTAGE SELECTOR	21793	410727
Q1	200247	TRANS FET DUAL	21793	200247
Q2	200200	TRANS NPN	21793	200200
Q3	200200	TRANS NPN	21793	200200
Q4	200200	TRANS NPN	21793	200200
Q5	200200	TRANS NPN	21793	200200
Q6	200068	TRANS PNP	80131	2N4250
Q7	200200	TRANS NPN	21793	200200
Q8	200267	TRANS NPN 400 V	50857	DTN9000
Q9	200230	TRANS FET N-CHAN, SIL JUNCTION		E305
Q10	200281	TRANS FET P-CHANNEL FALLOUT 2N5463	04713	2N5463
Q11	200200	TRANS NPN	21793	200200
Q12	200245	TRANS PNP HIGH VOLTAGE	04713	MPS-A92
Q13	200068	TRANS PNP	80131	2N4250
Q15	200280	TRANS FET P-CHANNEL GRADED 2N5463	04713	2N5463
Q16	200280	TRANS FET P-CHANNEL GRADED 2N5463	04713	2N5463
Q17	200280	TRANS FET P-CHANNEL GRADED 2N5463	04713	2N5463
Q18	200200	TRANS NPN	21793	200200
Q19	200200	TRANS NPN	21793	200200
Q20	200233	TRANS SILICO NPN	04713	MPS-A42
Q21	200265	TRANS FET 2N5951	01295	2N5951
Q22	200200	TRANS NPN	21793	200200
Q23	200139	TRANS POWER	01295	TIP30
R2	012081	RES METAL FILM 47.5 K 1% 1/8W	81349	RN55C4752F
R3	010838	RES CARBON 100 K 2% 1W	91637	SBF100K2%
R4	000221	RES CARBON 220 OHM 5% 1/4W	81349	RC07GF221J
R5	000305	RES CARBON 3 M 5% 1/4W	81349	RC07GF305J

401659 – Assy., PCB, MOTHERBOARD continued

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
R6	012095	RES, METAL FILM 37.4 K MATCHED PR .1% 1/10W	14298	UAR-1/10 C-6
R7	012095	RES, METAL FILM 37.4 K MATCHED PR .1% 1/10W	14298	UAR-1/10 C-6
R8	010829	RES METAL 4.99 K 1% 1/10W	81349	RN55C4991F
R9	012064	RES SET 100K/117 K MF 0.1%	03888	A3DR24
R10	000223	RES CARBON 22 K 5% 1/4W	81349	RC07GF223J
R11	000223	RES CARBON 22 K 5% 1/4W	81349	RC07GF223J
R13	000241	RES CARBON 240 OHM 5% 1/4W	81349	RC07GF241J
R14	000103	RES CARBON 10 K 5% 1/4W	81349	RC07GF103J
R15	000391	RES CARBON 390 OHM 5% 1/4W	81349	RC07GF391J
R16	000223	RES CARBON 22 K 5% 1/4W	81349	RC07GF223J
R17	000205	RES CARBON 2 M 5% 1/4W	81349	RC07GF205J
R18	000223	RES CARBON 22 K 5% 1/4W	81349	RC07GF223J
R19	000221	RES CARBON 220 OHM 5% 1/4W	81349	RC07GF221J
R20	010679	RES METAL 75 K 1% 1/10W	81349	RN55C7502F
R21	000223	RES CARBON 22 K 5% 1/4W	81349	RC07GF223J
R22	012064	RES SET 100K/117 K MF 0.1%	03888	A3DR24
R23	000223	RES CARBON 22 K 5% 1/4W	81349	RC07GF223J
R24	000104	RES CARBON 100 K 5% 1/4W	81349	RC07GF104J
R25	012093	RES, METAL FILM 90 K 1% 1 W	14298	PME70T-B
R26	001816	RES CARBON 47 K 5% 2W	01121	See Description
R27	012092	RES, METAL FILM 900 K 1% 1/4 W	14298	UAR-1/4 C-6
R28	012090	RES, METAL FILM 9 K 1% 1/10W	14298	UAR-1/10 C-6
R29	012088	RES, METAL FILM 1 K OHM 1% 1/10W	14298	UAR-1/10 C6
R30	000153	RES CARBON 15 K 5% 1/4W	81349	RC07GF153J
R31	012089	RES, METAL FILM 6.98 K 1% 1/10W	14298	UAR-1/10 C6
R32	000104	RES CARBON 100 K 5% 1/4W	81349	RC07GF104J
R33	012094	RES, METAL FILM 9 M 1% 1 W	03888	PME70T-B
R34	010723	RES METAL 4.42 K 1% 1/10W	81349	RN55C4421F
R35	012091	RES, METAL FILM 787 OHM 1% 1/4 W	14298	UAR-1/10 C-6
R37	000123	RES CARBON 12 K 5% 1/4W	81349	RC07GF123J
R38	000362	RES CARBON 3.6 K 5% 1/4W	81349	RC07GF362J
R39	000184	RES CARBON 180 K 5% 1/4W	81349	RC07GF184J
R40	000753	RES CARBON 75 K 5% 1/4W	81349	RC07GF753J
R41	010704	RES METAL 1 K 1% 1/10W	81349	RN55D1001F
R42	001783	RES CARBON 390 OHM 5% 1/2W	81349	RC20GF391J
R43	001783	RES CARBON 390 OHM 5% 1/2W	81349	RC20GF391J
R44	010536	RES METAL 100 K 1% 1/10W	81349	RN55C1003F
R45	010621	RES METAL 49.9 K 1% 1/10W	81349	RN55C4992F
R46	012065	RES SET 9.9M/100 K 0.1%	03888	A3DR25
R47	000102	RES CARBON 1 K 5% 1/4W	81349	RC07GF102J
R48	030015	RES WW 100 K 1% 10W	21551	M-100
R49	000181	RES CARBON 180 OHM 5% 1/4W	81349	RC07GF181J

401659 – Assy., PCB, MOTHERBOARD continued

REF DES	RACAL-DANA P/N	DESCRIPTION					FSC	MANU P/N
R50	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R51	012065	RES	SET	9.9M/100 K	MF	0.1%	03888	A3DR25
R52	001873	RES	CARBON	20 K		5% 2W	01121	See Description
R53	040305	POT	CERMET	100 K			73138	68WR100K
R54	000104	RES	CARBON	100 K		5% 1/4W	81349	RC07GF104J
R55	010686	RES	METAL	909 OHM		1% 1/10W	81349	RN55C9090F
R56	012063	RES	SET	100/900/9 K	MF	0.1%	03888	A3DR23
R57	000123	RES	CARBON	12 K		5% 1/4W	81349	RC07GF123J
R58	001676	RES	CARBON	10 K		5% 1/2W	81349	RC20GF103J
R59	000107	RES	CARBON	100 M		5% 1/4W	81349	RC07GF107J
R60	010621	RES	METAL	49.9 K		1% 1/10W	81349	RN55C4992F
R61	000107	RES	CARBON	100 M		5% 1/4W	81349	RC07GF107J
R62	000104	RES	CARBON	100 K		5% 1/4W	81349	RC07GF104J
R63	010137	RES	METAL	100 OHM	T-0	1% 1/8W	81349	RN60D1000F
R64	000123	RES	CARBON	12 K		5% 1/4W	81349	RC07GF123J
R65	000104	RES	CARBON	100 K		5% 1/4W	81349	RC07GF104J
R66	010704	RES	METAL	1 K		1% 1/10W	81349	RN55D1001F
R67	012063	RES	SET	100/900/9 K	MF	0.1%	03888	A3DR23
R68	012063	RES	SET	100/900/9 K	MF	0.1%	03888	A3DR23
R69	000123	RES	CARBON	12 K		5% 1/4W	81349	RC07GF123J
R70	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R71	001676	RES	CARBON	10 K		5% 1/2W	81349	RC20GF103J
R72	010529	RES	METAL	10 K		1% 1/10W	81349	RN55C1002F
R73	010704	RES	METAL	1 K		1% 1/10W	81349	RN55D1001F
R74	010621	RES	METAL	49.9 K		1% 1/10W	81349	RN55C4992F
R75	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R76	000473	RES	CARBON	47 K		5% 1/4W	81349	RC07GF473J
R77	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R79	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R80	000102	RES	CARBON	1 K		5% 1/4W	81349	RC07GF102J
R81	000152	RES	CARBON	1.5 K		5% 1/4W	81349	RC07GF152J
R82	001874	RES	CARBON	680 OHM		5% 1/2W	81349	RC20GF681J
R91	000471	RES	CARBON	470 OHM		5% 1/4W	81349	RC07GF471J
R92	000471	RES	CARBON	470 OHM		5% 1/4W	81349	RC07GF471J
R93	000103	RES	CARBON	10 K		5% 1/4W	81349	RC07GF103J
R94	000103	RES	CARBON	10 K		5% 1/4 W	81349	RC07GF103J
R95	010643	RES	METAL	71.5 K		1% 1/10W	81349	RN55C7152F
R96	010697	RES	METAL	26.7 K		1% 1/10W	81349	RN55C2672F
S1	600926	SWITCH, SLIDE PUSHBUTTON, MOMENTARY, Single, 2 Pole					71590	PBI Series
S2	600975	SWITCH, PUSHBUTTON					71590	SPEC-PB12.5
S201	600814	SWITCH		6 SPST			11237	206-6
T1	300097	TRANS	POWER					CMI-2570

401659 – Assy., PCB, MOTHERBOARD continued

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
TP1	600786	POST, MACHINE APPLIED STRIP	00779	1-87022-0
TP2	600786	POST, MACHINE APPLIED STRIP	00779	1-87022-0
TP3	600786	POST, MACHINE APPLIED STRIP	00779	1-87022-0
TP4	600786	POST, MACHINE APPLIED STRIP	00779	1-87022-0
TP5	600786	POST, MACHINE APPLIED STRIP	00779	1-87022-0
TP6	600786	POST, MACHINE APPLIED STRIP	00779	1-87022-0
TP7	600786	POST, MACHINE APPLIED STRIP	00779	1-87022-0
TP8	600786	POST, MACHINE APPLIED STRIP	00779	1-87022-0
TP9	600786	POST, MACHINE APPLIED STRIP	00779	1-87022-0
TP10	600786	POST, MACHINE APPLIED STRIP	00779	1-87022-0
TP11	600786	POST, MACHINE APPLIED STRIP	00779	1-87022-0
U1	230366	IC	27014	DM74LS174N
U2	230194	IC 14 DIP, DUAL D FLIP-FLOP	01295	SN74LS74N
U3	230461	IC TRANSISTOR ARRAY	02735	CA3096E
U5	230192	IC 14 DIP, INVERTER	01295	SN74LS05N
U6	230193	IC 14 DIP, NAND GATE	01295	SN74LS00N
U7	230336	IC	01295	74LS14
U8	230194	IC 14 DIP, DUAL D FLIP-FLOP	01295	SN74LS74N
U9	230460	IC HEX INVERTER	02735	CD4049BE
U10	230419	IC CUSTOM SPEC.	21793	230419
U11	230496	IC SELECTED LD120CJ	21793	230491
U12	230457	IC LED DRIVER ICM7218A	32293	ICM7218A
U13	230330	IC	01295	74LS367
U14	230368	IC	27014	74LS138
U15	230368	IC	27014	74LS138
U16	230330	IC	01295	74LS367
U17	230460	IC HEX INVERTER	02735	CD4049BE
U18	230464	IC RELAY DRIVER MC1416P	04713	MC1416P
U19	230464	IC RELAY DRIVER MC1416P	04713	MC1416P
U20	230330	IC	01295	74LS367
U21	230234	IC 14 DIP, HEX INVERTER	01295	SN74LS04N
U22	230537	IC MEMORY 2114	07263	2114
U23	230234	IC 14 DIP, HEX INVERTER	01295	SN74LS04N
U24	230248	IC POSITIVE NAND GATE	01295	SN74LS10N
U25	230629	IC DIGITAL 4093B	04713	4093B
U26	230468	IC ANALOG SWITCHES	01295	TL601CP
U27	230481	IC MEMORY ROM	21793	230481
U28	230495	IC MEMORY ROM	21793	230495
U31	230537	IC MEMORY 2114	07263	2114
U32	230356	IC	27014	74LS175
U33	230404	IC	02735	CD4094BE
U34	230404	IC	02735	CD4094BE
U35	230369	IC	04713	6802-P
U36	230471	IC 5 CHANNEL DRIVER	56289	UHP-490
U37	230402	IC	27014	74LS30N

401659 – Assy., PCB, MOTHERBOARD continued

REF DES	RACAL-DANA P/N	DESCRIPTION					FSC	MANU P/N
U38	230306	IC	QUAD, 2 INPUT NOR GATES				01295	SN74LS02
U39	230248	IC	POSITIVE NAND GATE				01295	SN74LS10N
U40	230194	IC	14 DIP, DUAL D FLIP-FLOP				01295	SN74LS74N
U41	230247	IC	MOS BILATERAL SWITCH				02735	CD4066AD
U42	230588	IC	DIGITALJAD NAND GATE				02735	CD4023UBE
U43	230455	IC	CMOS MEMORY				32293	IM6508
U44	230430	IC					04713	MC68488L
U45	230330	IC					01295	74LS367
U46	230459	IC	OCTAL GPIB TRANS			SN75160	01295	SN75160
U47	230472	IC	OCTAL GPIB TRANS			SN75161	01295	SN75161
U48	230200	IC					04713	MC7812-CT
U49	230378	IC					27014	7915CT
U50	230275	IC		5.0 V			04713	MC7805CT
U51	230275	IC		5.0 V			04713	MC7805CT
U52	230463	IC	+8 VOLT REGULATOR				04713	MC7808CT
U53	230515	IC	VOLTAGE DETECTOR, MICROPOWER				32293	ICL8212CPA
VR1	230453	IC	(+7V REFERENCE)				27014	LM399H
VR2	230454	IC	+7V REFERENCE				27014	LM3999Z
VR3	220088	DIODE	ZENER	30 V			04713	1N972B
VR4	220020	DIODE	SILICO, ZENER				81349	1N4370
VR5	220090	DIODE	ZENER				04713	1N4620
VR6	220035	DIODE	ZENER	16 V		5%	81349	1N966B
VR7	220011	DIODE	SILICO, ZENER				81349	1N751A
VR8	220060	DIODE	ZENER	24 V		5%	81349	1N970B
VR9	220060	DIODE	ZENER	24 V		5%	81349	1N970B
VR10	220040	DIODE	ZENER				81349	1N753A
VR11	220040	DIODE	ZENER				81349	1N753A
VR12	220019	DIODE	SILICO, ZENER				81349	1N752A
VR13	220088	DIODE	ZENER	30 V			04713	1N972B
VR14	220088	DIODE	ZENER	30 V			04713	1N972B
VR15	220015	DIODE	SILICO, ZENER				81349	1N967B
VR16	220015	DIODE	SILICO, ZENER				81349	1N967B
W1	600245	JUMPER, INSULATED						L-2007-1LP
W3	600245	JUMPER, INSULATED						L-2007-1LP
W4	600245	JUMPER, INSULATED						L-2007-1LP
W5	600245	JUMPER, INSULATED						L-2007-1LP
Y1	920846	CRYSTAL		2.4576 MHz				2.4576 MHz
Y2	920840	CRYSTAL		3.579 MHz				1107863-1
Z1	080011	RES	CERMET	1 K	Network 8P,7R	2%	11236	750-81-R1KΩ
Z2	080020	RES	CERMET	10 K	Network 8P,7R	2%	11236	750-81-R10KΩ
Z3	080030	RES	CERMET	22 K	Network 8P,7R	2%	11236	750-81-R22KΩ
Z4	080011	RES	CERMET	1 K	Network 8P,7R	2%	11236	750-81-R1KΩ
Z5	080020	RES	CERMET	10 K	Network 8P,7R	2%	11236	750-81-R10KΩ

401659 – Assy., PCB, MOTHERBOARD continued

REF DES	RACAL-DANA P/N	DESCRIPTION					FSC	MANU P/N
Z6	080001	RES	CERMET	330 OHM	Network 8P,7R	2%	11236	750-81-R330Ω
Z7	080020	RES	CERMET	10 K	Network 8P,7R	2%	11236	750-81-R10KΩ
Z8	080020	RES	CERMET	10 K	Network 8P,7R	2%	11236	750-81-R10KΩ
Z9	080020	RES	CERMET	10 K	Network 8P,7R	2%	11236	750-81-R10KΩ
Z10	080020	RES	CERMET	10 K	Network 8P,7R	2%	11236	750-81-R10KΩ

401651 – Assy., PCB, DISPLAY

REF DES	RACAL-DANA P/N	DESCRIPTION	FSC	MANU P/N
C1	110143	CAP TANTA 1 MFD 35 V 20%	05397	T368A105M035AS
C2	100062	CAP CERAM .01 MFD 100 V 10%	72982	8121-100-W5R0-103K
CR1	210072	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR2	210072	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR3	210072	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR4	210072	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR5	210072	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR6	210072	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR7	210072	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR8	210072	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR9	210072	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR10	210072	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR11	210072	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR12	210072	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR13	210072	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR14	210072	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR15	210072	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR16	210072	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR17	210072	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR18	210072	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR19	210072	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR20	210072	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR21	210072	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
CR22	210072	LAMP HI EFFICIENCY YELLOW - SOLID STATE	50434	HP5082-4550
DS1	210074	DIODE 7-SEGMENT LED DISPLAY, YELLOW	50434	HP5082-7660
DS2	210074	DIODE 7-SEGMENT LED DISPLAY, YELLOW	50434	HP5082-7660
DS3	210074	DIODE 7-SEGMENT LED DISPLAY, YELLOW	50434	HP5082-7660
DS4	210074	DIODE 7-SEGMENT LED DISPLAY, YELLOW	50434	HP5082-7660
DS5	210074	DIODE 7-SEGMENT LED DISPLAY, YELLOW	50434	HP5082-7660
DS6	210074	DIODE 7-SEGMENT LED DISPLAY, YELLOW	50434	HP5082-7660
DS7	210074	DIODE 7-SEGMENT LED DISPLAY, YELLOW	50434	HP5082-7660
J3	600228	CONN 18 P	71785	252-18-30-160
R1	001895	RES CC 4.3 OHMS 5% 1/4W	81349	RC07GF4R3J
R2	001895	RES CC 4.3 OHMS 5% 1/4W	81349	RC07GF4R3J
R3	001895	RES CC 4.3 OHMS 5% 1/4W	81349	RC07GF4R3J
R4	001895	RES CC 4.3 OHMS 5% 1/4W	81349	RC07GF4R3J
R5	001895	RES CC 4.3 OHMS 5% 1/4W	81349	RC07GF4R3J
R6	001895	RES CC 4.3 OHMS 5% 1/4W	81349	RC07GF4R3J
R7	001895	RES CC 4.3 OHMS 5% 1/4W	81349	RC07GF4R3J
R8	001895	RES CC 4.3 OHMS 5% 1/4W	81349	RC07GF4R3J

401651 – Assy., PCB, DISPLAY continued

REF DES	RACAL-DANA P/N	DESCRIPTION					FSC	MANU P/N
U1	230483	IC	DRIVER		UDN-2981A		56289	UDN-2981A
U2	230105	IC					01295	SN7417
U3	230105	IC					01295	SN7417
Z1	080009	RES	CERMET	6.8 K	Network 16P,8R	2%	11236	761-3-R6.8K
Z2	080000	RES	CERMET	200 OHM	Network 8P,7R	2%	11236	750-81-R220Ω

404107 – Assy., PCB, AC CONVERTER

REF DES	DANA P/N	DESCRIPTION						FSC	MANU P/N
B1	920563	BEAD	SHIELDING		56-59065/4B			02114	56-59065/4B
B2	920563	BEAD	SHIELDING		56-59065/4B			02114	56-59065/4B
B3	920563	BEAD	SHIELDING		56-59065/4B			02114	56-59065/4B
C1	120280	CAP	MYLAR	.22 MFD	1000 V	10%		27556	ZA2J224K
C2	130146	CAP	TRIMMER	.25-1.5 PFD				74970	273-0001-002
C3	111148	CAP	ELECT	100 MFD	25 V			34553	ET101X025A5
C4	100023	CAP	CERAM	.01 MFD	100 V			71471	Type TTP
C5	100023	CAP	CERAM	.01 MFD	100 V			71471	Type TTP
C6	110023	CAP	TANTA	2.2 MFD	35 V	10%		05397	T310B225K035AS
C7	111148	CAP	ELECT	100 MFD	25 V			34553	ET101X025A5
C8	110154	CAP	TANTA	68 MFD	6 V	20%		05397	T368B686M006AS
C9	101644	CAP	CERAM	200 PFD	1000 V	20%		71471	GPDX5F201K
C10	110143	CAP	TANTA	1 MFD	35 V	20%		05397	T368A105M035AS
C12	101644	CAP	CERAM	200 PFD	1000 V	20%		71471	GPDX5F201K
C13	120300	CAP	MYLAR	1.5 MFD	100 V	20%		73445	C281AH/A1M5
C14	120300	CAP	MYLAR	1.5 MFD	100 V	20%		73445	C281AH/A1M5
C16	120300	CAP	MYLAR	1.5 MFD	100 V	20%		73445	C281AH/A1M5
C17	120300	CAP	MYLAR	1.5 MFD	100 V	20%		73445	C281AH/A1M5
C18	120290	CAP	MYLAR	.22 MFD	100 V	20%		73445	C281AH/A220K
C19	120290	CAP	MYLAR	.22 MFD	100 V	20%		73445	C281AH/A220K
C20	100080	CAP	CERAM	.05 MFD	100 V	20%		56289	C023A101L503M
C21	100068	CAP	CERAM	.02 MFD	100 V	20%		56289	C023B101H203M
C22	100023	CAP	CERAM	.01 MFD	100 V			71471	Type TTP
C23	110043	CAP	ELECT	22 MFD	25 V			34553	ET220X025A3
C24	100023	CAP	CERAM	.01 MFD	100 V			71471	Type TTP
C25	110043	CAP	ELECT	22 MFD	25 V			34553	ET220X025A3
C26	130146	CAP	TRIMMER	.25-1.5 PFD				74970	273-0001-002
C27	100096	CAP	CERAM	5.6 PFD	1000 V	5%		56289	C023B102E5R6D
C28	100050	CAP	CERAM	2.2 PFD	1000 V	5%		56289	C030B102S2R2D
C29	130124	CAP	TRIMMER	1.2 - 10 PFD	250 V			52763	R-TRIKO-122-09SD
C30	100100	CAP	CERAM	FSV	100100			21793	100100
C31	120153	CAP	POLY	47 PFD	125 V	10%		26625	611
C32	110043	CAP	ELECT	22 MFD	25 V			34553	ET220X025A3
C33	100100	CAP	CERAM	FSV	100100			21793	100100
C34	130148	CAP	TRIMMER	5-20 PFD	250 V			52763	R-TRIKO-122-09MG
C35	120316	CAP	POLY	680 PFD	630 V	5%		08257	KSO Series
C36	101145	CAP	CERAM	100 PFD	500 V	10%		04222	TCD-DI-1N5600-100
C37	120135	CAP	POLY	.015 MFD	33 V	10%		26625	611.3S
C38	100023	CAP	CERAM	.01 MFD	100 V			71471	Type TTP

404107 – Assy., PCB, AC CONVERTER *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
CR1	210015	DIODE HP5082-2800	50434	HP5082-2800
CR2	210015	DIODE HP5082-2800	50434	HP5082-2800
CR3	210015	DIODE HP5082-2800	50434	HP5082-2800
CR4	210015	DIODE HP5082-2800	50434	HP5082-2800
CR5	211083	DIODE SILICO	81349	1N916B
CR6	211083	DIODE SILICO	81349	1N916B
CR7	211083	DIODE SILICO	81349	1N916B
CR8	220022	DIODE SILICO ZENER	81349	1N965B
CR9	220022	DIODE SILICO ZENER	81349	1N965B
CR10	220022	DIODE SILICO ZENER	81349	1N965B
CR11	211083	DIODE SILICO	81349	1N916B
K1	310148	RELAY REED 1 FORM A 12 V COIL	15636	R2699-2
K2	310148	RELAY REED 1 FORM A 12 V COIL	15636	R2699-2
K3	310148	RELAY REED 1 FORM A 12 V COIL	15636	R2699-2
Q1	200107	TRANS 2N4302	80131	2N4302
Q2	200163	TRANS SILICO NPN EN916	07263	EN916
Q3	200201	TRANS DUAL NPN 200201	21793	200201
Q4	200096	TRANS PNP 2N4917	81349	2N4917
Q5	200096	TRANS PNP 2N4917	81349	2N4917
Q6	200096	TRANS PNP 2N4917	81349	2N4917
Q7	200096	TRANS PNP 2N4917	81349	2N4917
Q8	200163	TRANS SILICO NPN EN916	07263	EN916
R1	010794	RES METAL MATCHED SET	21793	010794
R2	000513	RES CARBON 51 K 5% 1/4W	81349	RC07GF513J
R3	000363	RES CARBON 36 K 5% 1/4W	81349	RC07GF363J
R4	000104	RES CARBON 100 K 5% 1/4W	81349	RC07GF104J
R5	000472	RES CARBON 4.7 K 5% 1/4W	81349	RC07GF472J
R6	000363	RES CARBON 36 K 5% 1/4W	81349	RC07GF363J
R7	000433	RES CARBON 43 K 5% 1/4W	81349	RC07GF433J
R8	000202	RES CARBON 2 K 5% 1/4W	81349	RC07GF202J
R9	000242	RES CARBON 2.4 K 5% 1/4W	81349	RC07GF242J
R10	000361	RES CARBON 360 OHM 5% 1/4W	81349	RC07GF361J
R11	000270	RES CARBON 27 OHM 5% 1/4W	81349	RC07GF270J
R12	000362	RES CARBON 3.6 K 5% 1/4W	81349	RC07GF362J
R13	000242	RES CARBON 2.4 K 5% 1/4W	81349	RC07GF242J
R14	000223	RES CARBON 22 K 5% 1/4W	81349	RC07GF223J
R15	000245	RES CARBON 2.4 M 5% 1/4W	81349	RC07GF245J
R16	000361	RES CARBON 360 OHM 5% 1/4W	81349	RC07GF361J
R17	000562	RES CARBON 5.6 K 5% 1/4W	81349	RC07GF562J

404107 – Assy., PCB, AC CONVERTER *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R18	000433	RES	CARBON	43 K		5% 1/4W	81349	RC07GF433J
R19	040235	POT	CERMET	100 K		10%	73138	89PR100K
R20	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R21	000301	RES	CARBON	300 OHM		5% 1/4W	81349	RC07GF301J
R22	000270	RES	CARBON	27 OHM		5% 1/4W	81349	RC07GF270J
R23	000301	RES	CARBON	300 OHM		5% 1/4W	81349	RC07GF301J
R24	000331	RES	CARBON	330 OHM		5% 1/4W	81349	RC07GF331J
R28	010793	RES	METAL		MATCHED SET		21793	010793
R29	010793	RES	METAL		MATCHED SET		21793	010793
R30	010793	RES	METAL		MATCHED SET		21793	010793
R31	000101	RES	CARBON	100 OHM		5% 1/4W	81349	RC07GF101J
R32	000562	RES	CARBON	5.6 K		5% 1/4W	81349	RC07GF562J
R33	010744	RES	METAL	40 K	Pair with R34		21793	010744
R34	010744	RES	METAL	40 K	Pair with R33		21793	010744
R35	010744	RES	METAL	40 K	Pair with R36		21793	010744
R36	010744	RES	METAL	40 K	Pair with R35		21793	010744
R37	010743	RES	METAL	20 K	Pair with R38		21793	010743
R38	010743	RES	METAL	20 K	Pair with R37		21793	010743
R39	010792	RES	METAL	200 K	Pair with R40 .1%		21793	010792
R40	010792	RES	METAL	200 K	Pair with R39 .1%		21793	010792
R41	040233	POT	CERMET	20 K		10%	73138	89PR20K
R42	000100	RES	CARBON	10 OHM		5% 1/4W	81349	RC07GF100J
R43	000390	RES	CARBON	39 OHM		5% 1/4W	81349	RC07GF390J
R44	040229	POT	CERMET	1 K		10%	73138	89PR1K
R45	010643	RES	METAL	71.5 K		1% 1/10W	81349	RN55C7152F
R46	010794	RES	METAL		MATCHED SET		21793	010794
R47	040229	POT	CERMET	1 K		10%	73138	89PR1K
R48	010794	RES	METAL		MATCHED SET		21793	010794
R49	040226	POT	CERMET	100 OHM		10%	73138	89PR100
R50	010794	RES	METAL		MATCHED SET		21793	010794
R51	040230	POT	CERMET	2 K		10%	73138	89PR2K
R52	010795	RES	METAL	13.7 K		1% 1/10W	81349	RN55C1372F
R53	600245	JUMPER			L-2007-1LP			L-2007-1LP
R54	010794	RES	METAL		MATCHED SET		21793	010794
R55	001737	RES	CARBON	FSV	001737	5% 1/4W	21793	001737
U1	230127	INTEGRATED CIRCUIT			SSS725C		06665	SSS725C

404106 – Assy., PCB, RMS CONVERTER

REF DES	DANA P/N	DESCRIPTION						FSC	MANU P/N
B1	920563	BEADS	SHIELDING		56-59065/4B			02114	56-59065/4B
C1	130116	CAP	MICA	3900 PFD	500 V	2%		72136	DM19F392G0
C2	130160	CAP	MICA	330 PFD				72136	DM15 Series
C3	100097	CAP	CERAM	12 PFD	1000 V	5%		56289	C020B10E120J
C4	130124	CAP	TRIMMER	1.2 - 10 PFD	250 V			52763	R-TRIKO-122-09SD
C5	100081	CAP	CERAM	4.7 PFD	1000 V	5%		56289	C030B102E4R7D
C6	100054	CAP	CERAM	27 PFD	1000 V	5%		56289	C030B102G270J
C7	130123	CAP	TRIMMER	1-3 PFD	250 V			52763	R-TRIKO-122-09SD
C8	100095	CAP	CERAM	2.7±.5 PFD	1000 V			56289	C030B102S2R7D
C9	130146	CAP	TRIMMER	.25-1.5 PFD				74970	273-0001-002
C10	100017	CAP	CERAM	.01 MFD	100 V	20%		56289	C023B101F103M
C11	100017	CAP	CERAM	.01 MFD	100 V	20%		56289	C023B101F103M
C12	101098	CAP	CERAM	330 PFD	500 V	10%		56289	10TS-T33
C13	100051	CAP	CERAM	3 PFD	500 V			71471	TCD-B1-0
C14	101641	CAP	CERAM	470 PFD	500 V	10%		71471	SCD1X5F
C15	110140	CAP	TANTA	47 MFD	6 V	20%		05397	T368B476M006AS
C16	101641	CAP	CERAM	470 PFD	500 V	10%		71471	SCD1X5F
C17	101098	CAP	CERAM	330 PFD	500 V	10%		56289	10TS-T33
C18	130076	CAP	MICA	200 PFD	500 V	5%		72136	DM15-201J
C19	101642	CAP	CERAM	150 PFD	500 V	10%		71471	SCD1X5F
C20	120294	CAP	MYLAR	.47 MFD	100 V	20%		73445	C281AH/A470K
C21	120294	CAP	MYLAR	.47 MFD	100 V	20%		73445	C281AH/A470K
C22	120294	CAP	MYLAR	.47 MFD	100 V	20%		73445	C281AH/A470K
C23	110043	CAP	ELECT	22 MFD	25 V			34553	ET220X025A3
C24	110043	CAP	ELECT	22 MFD	25 V			34553	ET220X025A3
C25	120280	CAP	MYLAR	.22 MFD	1000 V	10%		27556	ZA2J224K
C26	100122	CAP	CERAM	1 PFD	1000 V	5%		72136	DM19F132J
C27	130146	CAP	TRIMMER	.25-1.5 PFD				74970	273-0001-002
C28	100017	CAP	CERAM	.01 MFD	100 V	20%		56289	C023B101F103M
C29	101641	CAP	CERAM	470 PFD	500 V	10%		71471	SCD1X5F
C30	100017	CAP	CERAM	.01 MFD	100 V	20%		56289	C023B101F103M
C31	100084	CAP	CERAM	1.5 ± .5 PFD	1000 V			56289	C030B102S1R5D
C32	100017	CAP	CERAM	.01 MFD	100 V	20%		56289	C023B101F103M
C33	100017	CAP	CERAM	.01 MFD	100 V	20%		56289	C023B101F103M
CR1	210015	DIODE			HP5082-2800			50434	HP5082-2800
CR2	210015	DIODE			HP5082-2800			50434	HP5082-2800
CR3	211083	DIODE	SILICO					81349	1N916B
CR4	211083	DIODE	SILICO					81349	1N916B
CR5	211083	DIODE	SILICO					81349	1N916B
CR6	211083	DIODE	SILICO					81349	1N916B
CR7	211083	DIODE	SILICO					81349	1N916B
CR8	211083	DIODE	SILICO					81349	1N916B
CR9	220016	DIODE	SILICO	ZENER	1N964B			81349	1N964B
CR10	220016	DIODE	SILICO	ZENER	1N964B			81349	1N964B

404106 – Assy., PCB, RMS CONVERTER *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
K1	310148	RELAY 1 FORM A 12 V COIL	15636	R2699-2
K2	310148	RELAY 1 FORM A 12 V COIL	15636	R2699-2
K3	310148	RELAY 1 FORM A 12 V COIL	15636	R2699-2
Q1	200200	TRANS NPN 200200	21793	200200
Q2	200200	TRANS NPN 200200	21793	200200
Q3	200199	TRANS FET FM1302	27014	FM1302
Q4	200200	TRANS NPN 200200	21793	200200
Q5	200201	TRANS DUAL NPN 200201	21793	200201
Q6	200112	TRANS MATCHED PAIR	21793	200112
Q7	200112	TRANS MATCHED PAIR	21793	200112
Q8	200068	TRANS PNP 2N4250	80131	2N4250
Q9	200200	TRANS NPN 200200	21793	200200
Q10	403865	KIT MATCHED LOG TRANSISTOR	21793	403865
Q11	200220	TRANS DUAL 200220	21793	200220
Q12	200136	TRANS SILICO NPN 2N5963	81349	2N5963
Q13	200068	TRANS PNP 2N4250	80131	2N4250
Q14	403865	KIT MATCHED LOG TRANSISTOR	21793	403865
Q15	200197	TRANS SILICO NPN MPS-H10	04713	MPS-H10
Q16	200197	TRANS SILICO NPN MPS-H10	04713	MPS-H10
R1	010721	RES METAL MATCHED SET	21793	010721
R2	010720	RES METAL 9.09 K .25% 1/10W	81349	RN55C9091C
R3	040228	POT CERMET 500 OHM 10%	73138	89PR500
R4	000820	RES CARBON 82 OHM 5% 1/4W	81349	RC07GF820J
R5	010721	RES METAL MATCHED SET	21793	010721
R6	040225	POT CERMET 50 OHM 20%	73138	89PR50
R7	010721	RES METAL MATCHED SET	21793	010721
R8	040228	POT CERMET 500 OHM 10%	73138	89PR500
R9	010721	RES METAL MATCHED SET	21793	010721
R10	000242	RES CARBON 2.4 K 5% 1/4W	81349	RC07GF242J
R11	010678	RES METAL 60.4 K 1% 1/10W	81349	RN55C6042F
R12	040231	POT CERMET 5 K 10%	73138	89PR5K
R13	001737	RES CARBON FSV 5% 1/4W	21793	001737
R14	010678	RES METAL 60.4 K 1% 1/10W	81349	RN55C6042F
R15	000101	RES CARBON 100 OHM 5% 1/4W	81349	RC07GF101J
R16	000334	RES CARBON 330 K 5% 1/4W	81349	RC07GF334J
R17	040235	POT CERMET 100 K 10%	73138	89PR100K
R18	000101	RES CARBON 100 OHM 5% 1/4W	81349	RC07GF101J
R19	010586	RES METAL 5 K .02%	18612	V53-1M
R20	000105	RES CARBON 1 M 5% 1/4W	81349	RC07GF105J
R21	000512	RES CARBON 5.1 K 5% 1/4W	81349	RC07GF512J

404106 – Assy., PCB, RMS CONVERTER *continued*

REF DES	DANA P/N	DESCRIPTION					FSC	MANU P/N
R22	000101	RES	CARBON	100 OHM	5%	1/4W	81349	RC07GF101J
R23	010586	RES	METAL	5 K	.02%		18612	V53-1M
R24	010654	RES	METAL	20 K	.05%		18612	V53-1
R25	040235	POT	CERMET	100 K	10%		73138	89PR100K
R26	000184	RES	CARBON	180 K	5%	1/4W	81349	RC07GF184J
R27	010684	RES	METAL	487 OHM	1%	1/10W	81349	RN55E4870F
R28	040225	POT	CERMET	50 OHM	20%		73138	89PR50
R29	000101	RES	CARBON	100 OHM	5%	1/4W	81349	RC07GF101J
R30	000103	RES	CARBON	10 K	5%	1/4W	81349	RC07GF103J
R31	000272	RES	CARBON	2.7 K	5%	1/4W	81349	RC07GF272J
R32	010615	RES	METAL	10 K	.02%		18612	V53-1M
R33	040225	POT	CERMET	50 OHM	20%		73138	89PR50
R34	010684	RES	METAL	487 OHM	1%	1/10W	81349	RN55E4870F
R35	000101	RES	CARBON	100 OHM	5%	1/4W	81349	RC07GF101J
R36	000681	RES	CARBON	680 OHM	5%	1/4W	81349	RC07GF681J
R37	000476	RES	CARBON	47 M	5%	1/4W	81349	RC07GF476J
R38	040239	POT	CERMET	1 M	20%		73138	89PR1M
R39	000103	RES	CARBON	10 K	5%	1/4W	81349	RC07GF103J
R40	000470	RES	CARBON	47 OHM	5%	1/4W	81349	RC07GF470J
R41	040231	POT	CERMET	5 K	10%		73138	89PR5K
R42	010281	RES	METAL	FSV	1%		21793	010281
R43	010392	RES	METAL	20 K	.1%	1/10W	81349	RN55C2002B
R44	000332	RES	CARBON	3.3 K	5%	1/4W	81349	RC07GF332J
R45	000107	RES	CARBON	100 M	5%	1/4W	81349	RC07GF107J
R46	040235	POT	CERMET	100 K	10%		73138	89PR100K
R47	000104	RES	CARBON	100 K	5%	1/4W	81349	RC07GF104J
R48	001768	RES	CARBON	3.3 OHM	5%	1/4W	01121	See Descrpt.
R49	040225	POT	CERMET	50 OHM	20%		73138	89PR50
R50	020667	RES	WW	100 K	.1%	.15W	22045	J-110
R51	010654	RES	METAL	20 K	.05%		18612	V53-1
R52	010654	RES	METAL	20 K	.05%		18612	V53-1
R53	001737	RES	CARBON	FSV	5%	1/4W	21793	001737
R54	001737	RES	CARBON	FSV	5%	1/4W	21793	001737
R55	040227	POT	CERMET	200 OHM	10%		73138	89PR200
R56	010615	RES	METAL	10 K	.02%		18612	V53-1M
R57	010721	RES	METAL	MATCHED SET			21793	010721
R58	010618	RES	METAL	200 K	.25%	1/10W	81349	RN55C2003C
R59	403865	KIT	MATCHED LOG TRANSISTOR				21793	403865
R60	001737	RES	CARBON	FSV	5%	1/4W	21793	001737
R61	010496	RES	METAL	1 M	1%	1/8W	81349	RN60D1004F
R62	403865	KIT	MATCHED LOG TRANSISTOR				21793	403865
R63	000221	RES	CARBON	220 OHM	5%	1/4W	81349	RC07GF221J

404106 – Assy., PCB, RMS CONVERTER *continued*

REF DES	DANA P/N	DESCRIPTION	FSC	MANU P/N
R64	000221	RES CARBON 220 OHM 5% 1/4W	81349	RC07GF221J
R65	001737	RES CARBON FSV 5% 1/4W	21793	001737
R66	010536	RES METAL 100 K 1% 1/10W	81349	RN55C1003F
R67	000513	RES CARBON 51 K 5% 1/4W	81349	RC07GF513J
R68	010233	RES METAL 32.4 K 1% 1/8 W	81349	RN60D3242F
S1	600742	SWITCH SLIDE SPDT	79727	GS-111
S2	600742	SWITCH SLIDE SPDT	79727	GS-111
TP1	600591	POST TEST POINT 85931-6	00779	85931-6
TP2	600591	POST TEST POINT 85931-6	00779	85931-6
TP3	600591	POST TEST POINT 85931-6	00779	85931-6
TP4	600591	POST TEST POINT 85931-6	00779	85931-6
TP5	600591	POST TEST POINT 85931-6	00779	85931-6
AR1	230180	INTEGRATED CIRCUIT LM318H	27014	LM318H
AR2	230054	INTEGRATED CIRCUIT LM301A	27014	LM301A
W1	600245	JUMPER L-2007-1LP		L-2007-1LP
W2	600245	JUMPER L-2007-1LP		L-2007-1LP

REPAIR REQUEST FORM

To allow us to better understand your repair requests, we suggest you use the following outline and include a copy with your instrument to be sent to your local Racal-Dana repair facility.

Model Number ____________________ Options ____________________ Date ______________

Serial Number ________________________ P. O.# ____________________________________

Company Name ____

Address ____

City ____________________________________ State __________ Zip Code ____________

Contact ____________________________ Phone Number _______________________________

1. Describe, in detail, the problem and symptoms you are having.

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2. If you are using your unit on the bus, please list the program strings used, if possible.

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3. List all input levels, and frequencies this failure occurs.

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4. Indicate any repair work previously performed.

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5. Please give any additional information you feel would be beneficial in facilitating a faster repair time. (I. E., modifications, etc.)

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